include "/app/lib/freepdk45/trunk/ncsu\_basekit/models/hspice/tran\_models/models\_nom/NMOS\_VTL.inc"

include "/app/lib/freepdk45/trunk/ncsu\_basekit/models/hspice/tran\_models/models\_nom/PMOS\_VTL.inc"

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*Adder\_16b\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

// Part of 16b adder, 16b subtractor

// Library name: Project

// Cell name: Adder

// View name: schematic

subckt Adder A B Cin Cout Sum Vdd Vss

parameters wp=100n lp=50nm wn=50n ln=50n mult=1

M11 (Sum Cin net11 Vdd) PMOS\_VTL w=6\*wp l=lp as=100e-9\*wp ad=100e-9\*wp \

ps=200e-9+wp pd=200e-9+wp m=mult

M10 (net11 B net15 Vdd) PMOS\_VTL w=6\*wp l=lp as=100e-9\*wp ad=100e-9\*wp \

ps=200e-9+wp pd=200e-9+wp m=mult

M9 (net15 A Vdd Vdd) PMOS\_VTL w=6\*wp l=lp as=100e-9\*wp ad=100e-9\*wp \

ps=200e-9+wp pd=200e-9+wp m=mult

M8 (Sum Cout net32 Vdd) PMOS\_VTL w=4\*wp l=lp as=100e-9\*wp ad=100e-9\*wp \

ps=200e-9+wp pd=200e-9+wp m=mult

M7 (net32 Cin Vdd Vdd) PMOS\_VTL w=4\*wp l=lp as=100e-9\*wp ad=100e-9\*wp \

ps=200e-9+wp pd=200e-9+wp m=mult

M6 (net32 B Vdd Vdd) PMOS\_VTL w=4\*wp l=lp as=100e-9\*wp ad=100e-9\*wp \

ps=200e-9+wp pd=200e-9+wp m=mult

M5 (net32 A Vdd Vdd) PMOS\_VTL w=4\*wp l=lp as=100e-9\*wp ad=100e-9\*wp \

ps=200e-9+wp pd=200e-9+wp m=mult

M4 (Cout A net39 Vdd) PMOS\_VTL w=4\*wp l=lp as=100e-9\*wp ad=100e-9\*wp \

ps=200e-9+wp pd=200e-9+wp m=mult

M3 (Cout Cin net52 Vdd) PMOS\_VTL w=4\*wp l=lp as=100e-9\*wp ad=100e-9\*wp \

ps=200e-9+wp pd=200e-9+wp m=mult

M2 (net39 B Vdd Vdd) PMOS\_VTL w=4\*wp l=lp as=100e-9\*wp ad=100e-9\*wp \

ps=200e-9+wp pd=200e-9+wp m=mult

M1 (net52 B Vdd Vdd) PMOS\_VTL w=4\*wp l=lp as=100e-9\*wp ad=100e-9\*wp \

ps=200e-9+wp pd=200e-9+wp m=mult

M0 (net52 A Vdd Vdd) PMOS\_VTL w=4\*wp l=lp as=100e-9\*wp ad=100e-9\*wp \

ps=200e-9+wp pd=200e-9+wp m=mult

M23 (net56 A Vss Vss) NMOS\_VTL w=3\*wn l=ln as=100e-9\*wn ad=100e-9\*wn \

ps=200e-9+wn pd=200e-9+wn m=mult

M22 (net60 B net56 Vss) NMOS\_VTL w=3\*wn l=ln as=100e-9\*wn ad=100e-9\*wn \

ps=200e-9+wn pd=200e-9+wn m=mult

M21 (Sum Cin net60 Vss) NMOS\_VTL w=3\*wn l=ln as=100e-9\*wn ad=100e-9\*wn \

ps=200e-9+wn pd=200e-9+wn m=mult

M20 (net76 Cin Vss Vss) NMOS\_VTL w=2\*wn l=ln as=100e-9\*wn ad=100e-9\*wn \

ps=200e-9+wn pd=200e-9+wn m=mult

M19 (net76 B Vss Vss) NMOS\_VTL w=2\*wn l=ln as=100e-9\*wn ad=100e-9\*wn \

ps=200e-9+wn pd=200e-9+wn m=mult

M18 (net76 A Vss Vss) NMOS\_VTL w=2\*wn l=ln as=100e-9\*wn ad=100e-9\*wn \

ps=200e-9+wn pd=200e-9+wn m=mult

M17 (Sum Cout net76 Vss) NMOS\_VTL w=2\*wn l=ln as=100e-9\*wn ad=100e-9\*wn \

ps=200e-9+wn pd=200e-9+wn m=mult

M16 (net84 B Vss Vss) NMOS\_VTL w=2\*wn l=ln as=100e-9\*wn ad=100e-9\*wn \

ps=200e-9+wn pd=200e-9+wn m=mult

M15 (Cout A net84 Vss) NMOS\_VTL w=2\*wn l=ln as=100e-9\*wn ad=100e-9\*wn \

ps=200e-9+wn pd=200e-9+wn m=mult

M14 (net96 B Vss Vss) NMOS\_VTL w=2\*wn l=ln as=100e-9\*wn ad=100e-9\*wn \

ps=200e-9+wn pd=200e-9+wn m=mult

M13 (net96 A Vss Vss) NMOS\_VTL w=2\*wn l=ln as=100e-9\*wn ad=100e-9\*wn \

ps=200e-9+wn pd=200e-9+wn m=mult

M12 (Cout Cin net96 Vss) NMOS\_VTL w=2\*wn l=ln as=100e-9\*wn ad=100e-9\*wn \

ps=200e-9+wn pd=200e-9+wn m=mult

ends Adder

// End of subcircuit definition.

// Part of 16b adder, 16b subtractor

// Library name: Project

// Cell name: Adder\_8b

// View name: schematic

subckt Adder\_8b A0 A1 A2 A3 A4 A5 A6 A7 B0 B1 B2 B3 B4 B5 B6 B7 Cin Cout \

VDD VSS s0 s1 s2 s3 s4 s5 s6 s7

I7 (A7 B7 net38 Cout s7 VDD VSS) Adder

I6 (A6 B6 net45 net38 s6 VDD VSS) Adder

I5 (A5 B5 net52 net45 s5 VDD VSS) Adder

I4 (A4 B4 net59 net52 s4 VDD VSS) Adder

I3 (A3 B3 net66 net59 s3 VDD VSS) Adder

I2 (A2 B2 net73 net66 s2 VDD VSS) Adder

I1 (A1 B1 net80 net73 s1 VDD VSS) Adder

I0 (A0 B0 Cin net80 s0 VDD VSS) Adder

ends Adder\_8b

// End of subcircuit definition.

// Part of 16b adder, 16b subtractor

// Library name: Project

// Cell name: ece3663Inverter\_1b

// View name: schematic

subckt ece3663Inverter\_1b VDD VSS in out

parameters wp=100n lp=50nm wn=50n ln=50n mult=1

MN (out in VSS VSS) NMOS\_VTL w=wn l=ln as=100e-9\*wn ad=100e-9\*wn \

ps=200e-9+wn pd=200e-9+wn ld=105n ls=105n m=mult

MP (out in VDD VDD) PMOS\_VTL w=wp l=lp as=100e-9\*wp ad=100e-9\*wp \

ps=200e-9+wp pd=200e-9+wp ld=105n ls=105n m=mult

ends ece3663Inverter\_1b

// End of subcircuit definition.

// Library name: Project

// Cell name: Adder\_16b

// View name: schematic

subckt Adder\_16b A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 B0 \

B1 B2 B3 B4 B5 B6 B7 B8 B9 B10 B11 B12 B13 B14 B15 Cin Cout S0 S1 \

S2 S3 S4 S5 S6 S7 S8 S9 S10 S11 S12 S13 S14 S15 Vdd Vss

I1 (A8 net64 A10 net66 A12 net130 A14 net126 B8 net72 B10 net74 B12 \

net76 B14 net78 net82 Cout Vdd Vss net191 S9 net187 S11 net183 S13 \

net179 S15) Adder\_8b

I0 (A0 net92 A2 net94 A4 net162 A6 net158 B0 net100 B2 net102 B4 \

net104 B6 net106 Cin net82 Vdd Vss net207 S1 net203 S3 net199 S5 \

net195 S7) Adder\_8b

I26 (Vdd Vss B15 net78) ece3663Inverter\_1b

I25 (Vdd Vss B13 net76) ece3663Inverter\_1b

I24 (Vdd Vss B11 net74) ece3663Inverter\_1b

I23 (Vdd Vss B9 net72) ece3663Inverter\_1b

I22 (Vdd Vss A15 net126) ece3663Inverter\_1b

I21 (Vdd Vss A13 net130) ece3663Inverter\_1b

I20 (Vdd Vss A11 net66) ece3663Inverter\_1b

I19 (Vdd Vss A9 net64) ece3663Inverter\_1b

I18 (Vdd Vss B7 net106) ece3663Inverter\_1b

I17 (Vdd Vss B5 net104) ece3663Inverter\_1b

I16 (Vdd Vss B3 net102) ece3663Inverter\_1b

I15 (Vdd Vss B1 net100) ece3663Inverter\_1b

I14 (Vdd Vss A7 net158) ece3663Inverter\_1b

I13 (Vdd Vss A5 net162) ece3663Inverter\_1b

I12 (Vdd Vss A3 net94) ece3663Inverter\_1b

I27 (Vdd Vss A1 net92) ece3663Inverter\_1b

I28 (Vdd Vss net179 S14) ece3663Inverter\_1b

I8 (Vdd Vss net183 S12) ece3663Inverter\_1b

I7 (Vdd Vss net187 S10) ece3663Inverter\_1b

I6 (Vdd Vss net191 S8) ece3663Inverter\_1b

I5 (Vdd Vss net195 S6) ece3663Inverter\_1b

I4 (Vdd Vss net199 S4) ece3663Inverter\_1b

I3 (Vdd Vss net203 S2) ece3663Inverter\_1b

I2 (Vdd Vss net207 S0) ece3663Inverter\_1b

ends Adder\_16b

// End of subcircuit definition.

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*Subtractor\_16b\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

// Library name: Project

// Cell name: Subtractor\_16b

// View name: schematic

subckt Subtractor\_16b A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 \

A15 B0 B1 B2 B3 B4 B5 B6 B7 B8 B9 B10 B11 B12 B13 B14 B15 Cout S0 \

S1 S2 S3 S4 S5 S6 S7 S8 S9 S10 S11 S12 S13 S14 S15 Vdd Vss

I1 (A8 net64 A10 net66 A12 net130 A14 net126 net72 B9 net74 B11 net76 \

B13 net78 B15 net82 Cout Vdd Vss net191 S9 net187 S11 net183 S13 \

net179 S15) Adder\_8b

I0 (A0 net92 A2 net94 A4 net162 A6 net158 net100 B1 net102 B3 net104 \

B5 net106 B7 Vdd net82 Vdd Vss net207 S1 net203 S3 net199 S5 \

net195 S7) Adder\_8b

I26 (Vdd Vss B14 net78) ece3663Inverter\_1b

I25 (Vdd Vss B12 net76) ece3663Inverter\_1b

I24 (Vdd Vss B10 net74) ece3663Inverter\_1b

I23 (Vdd Vss B8 net72) ece3663Inverter\_1b

I22 (Vdd Vss A15 net126) ece3663Inverter\_1b

I21 (Vdd Vss A13 net130) ece3663Inverter\_1b

I20 (Vdd Vss A11 net66) ece3663Inverter\_1b

I19 (Vdd Vss A9 net64) ece3663Inverter\_1b

I18 (Vdd Vss B6 net106) ece3663Inverter\_1b

I17 (Vdd Vss B4 net104) ece3663Inverter\_1b

I16 (Vdd Vss B2 net102) ece3663Inverter\_1b

I15 (Vdd Vss B0 net100) ece3663Inverter\_1b

I14 (Vdd Vss A7 net158) ece3663Inverter\_1b

I13 (Vdd Vss A5 net162) ece3663Inverter\_1b

I12 (Vdd Vss A3 net94) ece3663Inverter\_1b

I27 (Vdd Vss A1 net92) ece3663Inverter\_1b

I28 (Vdd Vss net179 S14) ece3663Inverter\_1b

I8 (Vdd Vss net183 S12) ece3663Inverter\_1b

I7 (Vdd Vss net187 S10) ece3663Inverter\_1b

I6 (Vdd Vss net191 S8) ece3663Inverter\_1b

I5 (Vdd Vss net195 S6) ece3663Inverter\_1b

I4 (Vdd Vss net199 S4) ece3663Inverter\_1b

I3 (Vdd Vss net203 S2) ece3663Inverter\_1b

I2 (Vdd Vss net207 S0) ece3663Inverter\_1b

ends Subtractor\_16b

// End of subcircuit definition.

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*AND\_16b\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

// Library name: Project

// Cell name: ece3663Inverter\_16b

// View name: schematic

subckt ece3663Inverter\_16b VDD VSS in\<15\> in\<14\> in\<13\> in\<12\> \

in\<11\> in\<10\> in\<9\> in\<8\> in\<7\> in\<6\> in\<5\> in\<4\> \

in\<3\> in\<2\> in\<1\> in\<0\> out\<15\> out\<14\> out\<13\> \

out\<12\> out\<11\> out\<10\> out\<9\> out\<8\> out\<7\> out\<6\> \

out\<5\> out\<4\> out\<3\> out\<2\> out\<1\> out\<0\>

parameters wp=90n wn=90n ln=50n lp=50n mult=1

MN\<15\> (out\<15\> in\<15\> VSS VSS) NMOS\_VTL w=wn l=ln as=100e-9\*wn \

ad=100e-9\*wn ps=200e-9+wn pd=200e-9+wn m=mult

MN\<14\> (out\<14\> in\<14\> VSS VSS) NMOS\_VTL w=wn l=ln as=100e-9\*wn \

ad=100e-9\*wn ps=200e-9+wn pd=200e-9+wn m=mult

MN\<13\> (out\<13\> in\<13\> VSS VSS) NMOS\_VTL w=wn l=ln as=100e-9\*wn \

ad=100e-9\*wn ps=200e-9+wn pd=200e-9+wn m=mult

MN\<12\> (out\<12\> in\<12\> VSS VSS) NMOS\_VTL w=wn l=ln as=100e-9\*wn \

ad=100e-9\*wn ps=200e-9+wn pd=200e-9+wn m=mult

MN\<11\> (out\<11\> in\<11\> VSS VSS) NMOS\_VTL w=wn l=ln as=100e-9\*wn \

ad=100e-9\*wn ps=200e-9+wn pd=200e-9+wn m=mult

MN\<10\> (out\<10\> in\<10\> VSS VSS) NMOS\_VTL w=wn l=ln as=100e-9\*wn \

ad=100e-9\*wn ps=200e-9+wn pd=200e-9+wn m=mult

MN\<9\> (out\<9\> in\<9\> VSS VSS) NMOS\_VTL w=wn l=ln as=100e-9\*wn \

ad=100e-9\*wn ps=200e-9+wn pd=200e-9+wn m=mult

MN\<8\> (out\<8\> in\<8\> VSS VSS) NMOS\_VTL w=wn l=ln as=100e-9\*wn \

ad=100e-9\*wn ps=200e-9+wn pd=200e-9+wn m=mult

MN\<7\> (out\<7\> in\<7\> VSS VSS) NMOS\_VTL w=wn l=ln as=100e-9\*wn \

ad=100e-9\*wn ps=200e-9+wn pd=200e-9+wn m=mult

MN\<6\> (out\<6\> in\<6\> VSS VSS) NMOS\_VTL w=wn l=ln as=100e-9\*wn \

ad=100e-9\*wn ps=200e-9+wn pd=200e-9+wn m=mult

MN\<5\> (out\<5\> in\<5\> VSS VSS) NMOS\_VTL w=wn l=ln as=100e-9\*wn \

ad=100e-9\*wn ps=200e-9+wn pd=200e-9+wn m=mult

MN\<4\> (out\<4\> in\<4\> VSS VSS) NMOS\_VTL w=wn l=ln as=100e-9\*wn \

ad=100e-9\*wn ps=200e-9+wn pd=200e-9+wn m=mult

MN\<3\> (out\<3\> in\<3\> VSS VSS) NMOS\_VTL w=wn l=ln as=100e-9\*wn \

ad=100e-9\*wn ps=200e-9+wn pd=200e-9+wn m=mult

MN\<2\> (out\<2\> in\<2\> VSS VSS) NMOS\_VTL w=wn l=ln as=100e-9\*wn \

ad=100e-9\*wn ps=200e-9+wn pd=200e-9+wn m=mult

MN\<1\> (out\<1\> in\<1\> VSS VSS) NMOS\_VTL w=wn l=ln as=100e-9\*wn \

ad=100e-9\*wn ps=200e-9+wn pd=200e-9+wn m=mult

MN\<0\> (out\<0\> in\<0\> VSS VSS) NMOS\_VTL w=wn l=ln as=100e-9\*wn \

ad=100e-9\*wn ps=200e-9+wn pd=200e-9+wn m=mult

MP\<15\> (out\<15\> in\<15\> VDD VDD) PMOS\_VTL w=wp l=lp as=100e-9\*wp \

ad=100e-9\*wp ps=200e-9+wp pd=200e-9+wp m=mult

MP\<14\> (out\<14\> in\<14\> VDD VDD) PMOS\_VTL w=wp l=lp as=100e-9\*wp \

ad=100e-9\*wp ps=200e-9+wp pd=200e-9+wp m=mult

MP\<13\> (out\<13\> in\<13\> VDD VDD) PMOS\_VTL w=wp l=lp as=100e-9\*wp \

ad=100e-9\*wp ps=200e-9+wp pd=200e-9+wp m=mult

MP\<12\> (out\<12\> in\<12\> VDD VDD) PMOS\_VTL w=wp l=lp as=100e-9\*wp \

ad=100e-9\*wp ps=200e-9+wp pd=200e-9+wp m=mult

MP\<11\> (out\<11\> in\<11\> VDD VDD) PMOS\_VTL w=wp l=lp as=100e-9\*wp \

ad=100e-9\*wp ps=200e-9+wp pd=200e-9+wp m=mult

MP\<10\> (out\<10\> in\<10\> VDD VDD) PMOS\_VTL w=wp l=lp as=100e-9\*wp \

ad=100e-9\*wp ps=200e-9+wp pd=200e-9+wp m=mult

MP\<9\> (out\<9\> in\<9\> VDD VDD) PMOS\_VTL w=wp l=lp as=100e-9\*wp \

ad=100e-9\*wp ps=200e-9+wp pd=200e-9+wp m=mult

MP\<8\> (out\<8\> in\<8\> VDD VDD) PMOS\_VTL w=wp l=lp as=100e-9\*wp \

ad=100e-9\*wp ps=200e-9+wp pd=200e-9+wp m=mult

MP\<7\> (out\<7\> in\<7\> VDD VDD) PMOS\_VTL w=wp l=lp as=100e-9\*wp \

ad=100e-9\*wp ps=200e-9+wp pd=200e-9+wp m=mult

MP\<6\> (out\<6\> in\<6\> VDD VDD) PMOS\_VTL w=wp l=lp as=100e-9\*wp \

ad=100e-9\*wp ps=200e-9+wp pd=200e-9+wp m=mult

MP\<5\> (out\<5\> in\<5\> VDD VDD) PMOS\_VTL w=wp l=lp as=100e-9\*wp \

ad=100e-9\*wp ps=200e-9+wp pd=200e-9+wp m=mult

MP\<4\> (out\<4\> in\<4\> VDD VDD) PMOS\_VTL w=wp l=lp as=100e-9\*wp \

ad=100e-9\*wp ps=200e-9+wp pd=200e-9+wp m=mult

MP\<3\> (out\<3\> in\<3\> VDD VDD) PMOS\_VTL w=wp l=lp as=100e-9\*wp \

ad=100e-9\*wp ps=200e-9+wp pd=200e-9+wp m=mult

MP\<2\> (out\<2\> in\<2\> VDD VDD) PMOS\_VTL w=wp l=lp as=100e-9\*wp \

ad=100e-9\*wp ps=200e-9+wp pd=200e-9+wp m=mult

MP\<1\> (out\<1\> in\<1\> VDD VDD) PMOS\_VTL w=wp l=lp as=100e-9\*wp \

ad=100e-9\*wp ps=200e-9+wp pd=200e-9+wp m=mult

MP\<0\> (out\<0\> in\<0\> VDD VDD) PMOS\_VTL w=wp l=lp as=100e-9\*wp \

ad=100e-9\*wp ps=200e-9+wp pd=200e-9+wp m=mult

ends ece3663Inverter\_16b

// End of subcircuit definition.

// Library name: Project

// Cell name: ece3663AND\_16b

// View name: schematic

subckt ece3663AND\_16b A\<15\> A\<14\> A\<13\> A\<12\> A\<11\> A\<10\> \

A\<9\> A\<8\> A\<7\> A\<6\> A\<5\> A\<4\> A\<3\> A\<2\> A\<1\> \

A\<0\> B\<15\> B\<14\> B\<13\> B\<12\> B\<11\> B\<10\> B\<9\> \

B\<8\> B\<7\> B\<6\> B\<5\> B\<4\> B\<3\> B\<2\> B\<1\> B\<0\> VDD \

VSS out\<15\> out\<14\> out\<13\> out\<12\> out\<11\> out\<10\> \

out\<9\> out\<8\> out\<7\> out\<6\> out\<5\> out\<4\> out\<3\> \

out\<2\> out\<1\> out\<0\>

parameters wp=90n wn=90n ln=50n lp=50n mult=1

MN1\<15\> (net6\<0\> B\<15\> VSS VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MN1\<14\> (net6\<1\> B\<14\> VSS VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MN1\<13\> (net6\<2\> B\<13\> VSS VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MN1\<12\> (net6\<3\> B\<12\> VSS VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MN1\<11\> (net6\<4\> B\<11\> VSS VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MN1\<10\> (net6\<5\> B\<10\> VSS VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MN1\<9\> (net6\<6\> B\<9\> VSS VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MN1\<8\> (net6\<7\> B\<8\> VSS VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MN1\<7\> (net6\<8\> B\<7\> VSS VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MN1\<6\> (net6\<9\> B\<6\> VSS VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MN1\<5\> (net6\<10\> B\<5\> VSS VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MN1\<4\> (net6\<11\> B\<4\> VSS VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MN1\<3\> (net6\<12\> B\<3\> VSS VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MN1\<2\> (net6\<13\> B\<2\> VSS VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MN1\<1\> (net6\<14\> B\<1\> VSS VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MN1\<0\> (net6\<15\> B\<0\> VSS VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MN0\<15\> (net14\<0\> A\<15\> net6\<0\> VSS) NMOS\_VTL w=wn l=ln \

as=9.45e-15 ad=9.45e-15 ps=300n pd=300n m=1

MN0\<14\> (net14\<1\> A\<14\> net6\<1\> VSS) NMOS\_VTL w=wn l=ln \

as=9.45e-15 ad=9.45e-15 ps=300n pd=300n m=1

MN0\<13\> (net14\<2\> A\<13\> net6\<2\> VSS) NMOS\_VTL w=wn l=ln \

as=9.45e-15 ad=9.45e-15 ps=300n pd=300n m=1

MN0\<12\> (net14\<3\> A\<12\> net6\<3\> VSS) NMOS\_VTL w=wn l=ln \

as=9.45e-15 ad=9.45e-15 ps=300n pd=300n m=1

MN0\<11\> (net14\<4\> A\<11\> net6\<4\> VSS) NMOS\_VTL w=wn l=ln \

as=9.45e-15 ad=9.45e-15 ps=300n pd=300n m=1

MN0\<10\> (net14\<5\> A\<10\> net6\<5\> VSS) NMOS\_VTL w=wn l=ln \

as=9.45e-15 ad=9.45e-15 ps=300n pd=300n m=1

MN0\<9\> (net14\<6\> A\<9\> net6\<6\> VSS) NMOS\_VTL w=wn l=ln \

as=9.45e-15 ad=9.45e-15 ps=300n pd=300n m=1

MN0\<8\> (net14\<7\> A\<8\> net6\<7\> VSS) NMOS\_VTL w=wn l=ln \

as=9.45e-15 ad=9.45e-15 ps=300n pd=300n m=1

MN0\<7\> (net14\<8\> A\<7\> net6\<8\> VSS) NMOS\_VTL w=wn l=ln \

as=9.45e-15 ad=9.45e-15 ps=300n pd=300n m=1

MN0\<6\> (net14\<9\> A\<6\> net6\<9\> VSS) NMOS\_VTL w=wn l=ln \

as=9.45e-15 ad=9.45e-15 ps=300n pd=300n m=1

MN0\<5\> (net14\<10\> A\<5\> net6\<10\> VSS) NMOS\_VTL w=wn l=ln \

as=9.45e-15 ad=9.45e-15 ps=300n pd=300n m=1

MN0\<4\> (net14\<11\> A\<4\> net6\<11\> VSS) NMOS\_VTL w=wn l=ln \

as=9.45e-15 ad=9.45e-15 ps=300n pd=300n m=1

MN0\<3\> (net14\<12\> A\<3\> net6\<12\> VSS) NMOS\_VTL w=wn l=ln \

as=9.45e-15 ad=9.45e-15 ps=300n pd=300n m=1

MN0\<2\> (net14\<13\> A\<2\> net6\<13\> VSS) NMOS\_VTL w=wn l=ln \

as=9.45e-15 ad=9.45e-15 ps=300n pd=300n m=1

MN0\<1\> (net14\<14\> A\<1\> net6\<14\> VSS) NMOS\_VTL w=wn l=ln \

as=9.45e-15 ad=9.45e-15 ps=300n pd=300n m=1

MN0\<0\> (net14\<15\> A\<0\> net6\<15\> VSS) NMOS\_VTL w=wn l=ln \

as=9.45e-15 ad=9.45e-15 ps=300n pd=300n m=1

MP0\<15\> (net14\<0\> A\<15\> VDD VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MP0\<14\> (net14\<1\> A\<14\> VDD VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MP0\<13\> (net14\<2\> A\<13\> VDD VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MP0\<12\> (net14\<3\> A\<12\> VDD VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MP0\<11\> (net14\<4\> A\<11\> VDD VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MP0\<10\> (net14\<5\> A\<10\> VDD VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MP0\<9\> (net14\<6\> A\<9\> VDD VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MP0\<8\> (net14\<7\> A\<8\> VDD VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MP0\<7\> (net14\<8\> A\<7\> VDD VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MP0\<6\> (net14\<9\> A\<6\> VDD VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MP0\<5\> (net14\<10\> A\<5\> VDD VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MP0\<4\> (net14\<11\> A\<4\> VDD VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MP0\<3\> (net14\<12\> A\<3\> VDD VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MP0\<2\> (net14\<13\> A\<2\> VDD VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MP0\<1\> (net14\<14\> A\<1\> VDD VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MP0\<0\> (net14\<15\> A\<0\> VDD VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MP1\<15\> (net14\<0\> B\<15\> VDD VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MP1\<14\> (net14\<1\> B\<14\> VDD VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MP1\<13\> (net14\<2\> B\<13\> VDD VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MP1\<12\> (net14\<3\> B\<12\> VDD VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MP1\<11\> (net14\<4\> B\<11\> VDD VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MP1\<10\> (net14\<5\> B\<10\> VDD VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MP1\<9\> (net14\<6\> B\<9\> VDD VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MP1\<8\> (net14\<7\> B\<8\> VDD VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MP1\<7\> (net14\<8\> B\<7\> VDD VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MP1\<6\> (net14\<9\> B\<6\> VDD VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MP1\<5\> (net14\<10\> B\<5\> VDD VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MP1\<4\> (net14\<11\> B\<4\> VDD VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MP1\<3\> (net14\<12\> B\<3\> VDD VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MP1\<2\> (net14\<13\> B\<2\> VDD VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MP1\<1\> (net14\<14\> B\<1\> VDD VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MP1\<0\> (net14\<15\> B\<0\> VDD VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

I0 (VDD VSS net14\<0\> net14\<1\> net14\<2\> net14\<3\> net14\<4\> \

net14\<5\> net14\<6\> net14\<7\> net14\<8\> net14\<9\> net14\<10\> \

net14\<11\> net14\<12\> net14\<13\> net14\<14\> net14\<15\> \

out\<15\> out\<14\> out\<13\> out\<12\> out\<11\> out\<10\> \

out\<9\> out\<8\> out\<7\> out\<6\> out\<5\> out\<4\> out\<3\> \

out\<2\> out\<1\> out\<0\>) ece3663Inverter\_16b

ends ece3663AND\_16b

// End of subcircuit definition.

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*OR\_16b\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

// Library name: Project

// Cell name: ece3663OR\_16b

// View name: schematic

subckt ece3663OR\_16b A\<15\> A\<14\> A\<13\> A\<12\> A\<11\> A\<10\> \

A\<9\> A\<8\> A\<7\> A\<6\> A\<5\> A\<4\> A\<3\> A\<2\> A\<1\> \

A\<0\> B\<15\> B\<14\> B\<13\> B\<12\> B\<11\> B\<10\> B\<9\> \

B\<8\> B\<7\> B\<6\> B\<5\> B\<4\> B\<3\> B\<2\> B\<1\> B\<0\> VDD \

VSS out\<15\> out\<14\> out\<13\> out\<12\> out\<11\> out\<10\> \

out\<9\> out\<8\> out\<7\> out\<6\> out\<5\> out\<4\> out\<3\> \

out\<2\> out\<1\> out\<0\>

parameters wp=90n wn=90n ln=50n lp=50n mult=1

MN1\<15\> (net10\<0\> B\<15\> VSS VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n ld=105n ls=105n m=1

MN1\<14\> (net10\<1\> B\<14\> VSS VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n ld=105n ls=105n m=1

MN1\<13\> (net10\<2\> B\<13\> VSS VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n ld=105n ls=105n m=1

MN1\<12\> (net10\<3\> B\<12\> VSS VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n ld=105n ls=105n m=1

MN1\<11\> (net10\<4\> B\<11\> VSS VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n ld=105n ls=105n m=1

MN1\<10\> (net10\<5\> B\<10\> VSS VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n ld=105n ls=105n m=1

MN1\<9\> (net10\<6\> B\<9\> VSS VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n ld=105n ls=105n m=1

MN1\<8\> (net10\<7\> B\<8\> VSS VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n ld=105n ls=105n m=1

MN1\<7\> (net10\<8\> B\<7\> VSS VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n ld=105n ls=105n m=1

MN1\<6\> (net10\<9\> B\<6\> VSS VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n ld=105n ls=105n m=1

MN1\<5\> (net10\<10\> B\<5\> VSS VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n ld=105n ls=105n m=1

MN1\<4\> (net10\<11\> B\<4\> VSS VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n ld=105n ls=105n m=1

MN1\<3\> (net10\<12\> B\<3\> VSS VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n ld=105n ls=105n m=1

MN1\<2\> (net10\<13\> B\<2\> VSS VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n ld=105n ls=105n m=1

MN1\<1\> (net10\<14\> B\<1\> VSS VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n ld=105n ls=105n m=1

MN1\<0\> (net10\<15\> B\<0\> VSS VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n ld=105n ls=105n m=1

MN0\<15\> (net10\<0\> A\<15\> VSS VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n ld=105n ls=105n m=1

MN0\<14\> (net10\<1\> A\<14\> VSS VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n ld=105n ls=105n m=1

MN0\<13\> (net10\<2\> A\<13\> VSS VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n ld=105n ls=105n m=1

MN0\<12\> (net10\<3\> A\<12\> VSS VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n ld=105n ls=105n m=1

MN0\<11\> (net10\<4\> A\<11\> VSS VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n ld=105n ls=105n m=1

MN0\<10\> (net10\<5\> A\<10\> VSS VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n ld=105n ls=105n m=1

MN0\<9\> (net10\<6\> A\<9\> VSS VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n ld=105n ls=105n m=1

MN0\<8\> (net10\<7\> A\<8\> VSS VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n ld=105n ls=105n m=1

MN0\<7\> (net10\<8\> A\<7\> VSS VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n ld=105n ls=105n m=1

MN0\<6\> (net10\<9\> A\<6\> VSS VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n ld=105n ls=105n m=1

MN0\<5\> (net10\<10\> A\<5\> VSS VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n ld=105n ls=105n m=1

MN0\<4\> (net10\<11\> A\<4\> VSS VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n ld=105n ls=105n m=1

MN0\<3\> (net10\<12\> A\<3\> VSS VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n ld=105n ls=105n m=1

MN0\<2\> (net10\<13\> A\<2\> VSS VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n ld=105n ls=105n m=1

MN0\<1\> (net10\<14\> A\<1\> VSS VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n ld=105n ls=105n m=1

MN0\<0\> (net10\<15\> A\<0\> VSS VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n ld=105n ls=105n m=1

MP1\<15\> (net14\<0\> B\<15\> VDD VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n ld=105n ls=105n m=1

MP1\<14\> (net14\<1\> B\<14\> VDD VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n ld=105n ls=105n m=1

MP1\<13\> (net14\<2\> B\<13\> VDD VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n ld=105n ls=105n m=1

MP1\<12\> (net14\<3\> B\<12\> VDD VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n ld=105n ls=105n m=1

MP1\<11\> (net14\<4\> B\<11\> VDD VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n ld=105n ls=105n m=1

MP1\<10\> (net14\<5\> B\<10\> VDD VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n ld=105n ls=105n m=1

MP1\<9\> (net14\<6\> B\<9\> VDD VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n ld=105n ls=105n m=1

MP1\<8\> (net14\<7\> B\<8\> VDD VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n ld=105n ls=105n m=1

MP1\<7\> (net14\<8\> B\<7\> VDD VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n ld=105n ls=105n m=1

MP1\<6\> (net14\<9\> B\<6\> VDD VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n ld=105n ls=105n m=1

MP1\<5\> (net14\<10\> B\<5\> VDD VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n ld=105n ls=105n m=1

MP1\<4\> (net14\<11\> B\<4\> VDD VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n ld=105n ls=105n m=1

MP1\<3\> (net14\<12\> B\<3\> VDD VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n ld=105n ls=105n m=1

MP1\<2\> (net14\<13\> B\<2\> VDD VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n ld=105n ls=105n m=1

MP1\<1\> (net14\<14\> B\<1\> VDD VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n ld=105n ls=105n m=1

MP1\<0\> (net14\<15\> B\<0\> VDD VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n ld=105n ls=105n m=1

MP0\<15\> (net10\<0\> A\<15\> net14\<0\> VDD) PMOS\_VTL w=wp l=lp \

as=9.45e-15 ad=9.45e-15 ps=300n pd=300n ld=105n ls=105n m=1

MP0\<14\> (net10\<1\> A\<14\> net14\<1\> VDD) PMOS\_VTL w=wp l=lp \

as=9.45e-15 ad=9.45e-15 ps=300n pd=300n ld=105n ls=105n m=1

MP0\<13\> (net10\<2\> A\<13\> net14\<2\> VDD) PMOS\_VTL w=wp l=lp \

as=9.45e-15 ad=9.45e-15 ps=300n pd=300n ld=105n ls=105n m=1

MP0\<12\> (net10\<3\> A\<12\> net14\<3\> VDD) PMOS\_VTL w=wp l=lp \

as=9.45e-15 ad=9.45e-15 ps=300n pd=300n ld=105n ls=105n m=1

MP0\<11\> (net10\<4\> A\<11\> net14\<4\> VDD) PMOS\_VTL w=wp l=lp \

as=9.45e-15 ad=9.45e-15 ps=300n pd=300n ld=105n ls=105n m=1

MP0\<10\> (net10\<5\> A\<10\> net14\<5\> VDD) PMOS\_VTL w=wp l=lp \

as=9.45e-15 ad=9.45e-15 ps=300n pd=300n ld=105n ls=105n m=1

MP0\<9\> (net10\<6\> A\<9\> net14\<6\> VDD) PMOS\_VTL w=wp l=lp \

as=9.45e-15 ad=9.45e-15 ps=300n pd=300n ld=105n ls=105n m=1

MP0\<8\> (net10\<7\> A\<8\> net14\<7\> VDD) PMOS\_VTL w=wp l=lp \

as=9.45e-15 ad=9.45e-15 ps=300n pd=300n ld=105n ls=105n m=1

MP0\<7\> (net10\<8\> A\<7\> net14\<8\> VDD) PMOS\_VTL w=wp l=lp \

as=9.45e-15 ad=9.45e-15 ps=300n pd=300n ld=105n ls=105n m=1

MP0\<6\> (net10\<9\> A\<6\> net14\<9\> VDD) PMOS\_VTL w=wp l=lp \

as=9.45e-15 ad=9.45e-15 ps=300n pd=300n ld=105n ls=105n m=1

MP0\<5\> (net10\<10\> A\<5\> net14\<10\> VDD) PMOS\_VTL w=wp l=lp \

as=9.45e-15 ad=9.45e-15 ps=300n pd=300n ld=105n ls=105n m=1

MP0\<4\> (net10\<11\> A\<4\> net14\<11\> VDD) PMOS\_VTL w=wp l=lp \

as=9.45e-15 ad=9.45e-15 ps=300n pd=300n ld=105n ls=105n m=1

MP0\<3\> (net10\<12\> A\<3\> net14\<12\> VDD) PMOS\_VTL w=wp l=lp \

as=9.45e-15 ad=9.45e-15 ps=300n pd=300n ld=105n ls=105n m=1

MP0\<2\> (net10\<13\> A\<2\> net14\<13\> VDD) PMOS\_VTL w=wp l=lp \

as=9.45e-15 ad=9.45e-15 ps=300n pd=300n ld=105n ls=105n m=1

MP0\<1\> (net10\<14\> A\<1\> net14\<14\> VDD) PMOS\_VTL w=wp l=lp \

as=9.45e-15 ad=9.45e-15 ps=300n pd=300n ld=105n ls=105n m=1

MP0\<0\> (net10\<15\> A\<0\> net14\<15\> VDD) PMOS\_VTL w=wp l=lp \

as=9.45e-15 ad=9.45e-15 ps=300n pd=300n ld=105n ls=105n m=1

I0 (VDD VSS net10\<0\> net10\<1\> net10\<2\> net10\<3\> net10\<4\> \

net10\<5\> net10\<6\> net10\<7\> net10\<8\> net10\<9\> net10\<10\> \

net10\<11\> net10\<12\> net10\<13\> net10\<14\> net10\<15\> \

out\<15\> out\<14\> out\<13\> out\<12\> out\<11\> out\<10\> \

out\<9\> out\<8\> out\<7\> out\<6\> out\<5\> out\<4\> out\<3\> \

out\<2\> out\<1\> out\<0\>) ece3663Inverter\_16b

ends ece3663OR\_16b

// End of subcircuit definition.

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*PASSA\_16b\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

// Library name: Project

// Cell name: ece3663PASSA\_16b

// View name: schematic

subckt ece3663PASSA\_16b A\<15\> A\<14\> A\<13\> A\<12\> A\<11\> A\<10\> \

A\<9\> A\<8\> A\<7\> A\<6\> A\<5\> A\<4\> A\<3\> A\<2\> A\<1\> \

A\<0\> VDD VSS out\<15\> out\<14\> out\<13\> out\<12\> out\<11\> \

out\<10\> out\<9\> out\<8\> out\<7\> out\<6\> out\<5\> out\<4\> \

out\<3\> out\<2\> out\<1\> out\<0\>

parameters wp=90n wn=90n ln=50n lp=50n mult=1

MN0\<15\> (A\<15\> VDD out\<15\> VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MN0\<14\> (A\<14\> VDD out\<14\> VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MN0\<13\> (A\<13\> VDD out\<13\> VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MN0\<12\> (A\<12\> VDD out\<12\> VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MN0\<11\> (A\<11\> VDD out\<11\> VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MN0\<10\> (A\<10\> VDD out\<10\> VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MN0\<9\> (A\<9\> VDD out\<9\> VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MN0\<8\> (A\<8\> VDD out\<8\> VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MN0\<7\> (A\<7\> VDD out\<7\> VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MN0\<6\> (A\<6\> VDD out\<6\> VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MN0\<5\> (A\<5\> VDD out\<5\> VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MN0\<4\> (A\<4\> VDD out\<4\> VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MN0\<3\> (A\<3\> VDD out\<3\> VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MN0\<2\> (A\<2\> VDD out\<2\> VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MN0\<1\> (A\<1\> VDD out\<1\> VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MN0\<0\> (A\<0\> VDD out\<0\> VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MP0\<15\> (A\<15\> VSS out\<15\> VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MP0\<14\> (A\<14\> VSS out\<14\> VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MP0\<13\> (A\<13\> VSS out\<13\> VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MP0\<12\> (A\<12\> VSS out\<12\> VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MP0\<11\> (A\<11\> VSS out\<11\> VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MP0\<10\> (A\<10\> VSS out\<10\> VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MP0\<9\> (A\<9\> VSS out\<9\> VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MP0\<8\> (A\<8\> VSS out\<8\> VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MP0\<7\> (A\<7\> VSS out\<7\> VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MP0\<6\> (A\<6\> VSS out\<6\> VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MP0\<5\> (A\<5\> VSS out\<5\> VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MP0\<4\> (A\<4\> VSS out\<4\> VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MP0\<3\> (A\<3\> VSS out\<3\> VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MP0\<2\> (A\<2\> VSS out\<2\> VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MP0\<1\> (A\<1\> VSS out\<1\> VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MP0\<0\> (A\<0\> VSS out\<0\> VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

ends ece3663PASSA\_16b

// End of subcircuit definition.

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*Shifter\_16b\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

//shifter netlist

subckt Inverter VDD VSS in out

parameters wp=90n wn=90n ln=50n lp=50n mult=1

MN (out in VSS VSS) NMOS\_VTL w=wn l=ln as=100e-9\*wn ad=100e-9\*wn ps=200e-9+wn pd=200e-9+wn ld=105n ls=105n m=mult

MP (out in VDD VDD) PMOS\_VTL w=wp l=lp as=100e-9\*wp ad=100e-9\*wp ps=200e-9+wp pd=200e-9+wp ld=105n ls=105n m=mult

ends Inverter

// NAND GATE

subckt NAND (VDD VSS A B out)

parameters wp=90n wn=180n lp=50n ln=50n mult=1

M0 (out A VDD VDD) PMOS\_VTL w=wp l=lp as=100n\*wp ad=100n\*wp ps=200n+wp pd=200n+wp m=mult

M1 (out B VDD VDD) PMOS\_VTL w=wp l=lp as=100n\*wp ad=100n\*wp ps=200n+wp pd=200n+wp m=mult

M2 (net5 B VSS VSS) NMOS\_VTL w=wn l=ln as=100n\*2\*wn ad=100n\*2\*wn ps=200n+2\*wn pd=200n+2\*wn m=mult

M3 (out A net5 VSS) NMOS\_VTL w=wn l=ln as=100n\*2\*wn ad=100n\*2\*wn ps=200n+2\*wn pd=200n+2\*wn m=mult

ends NAND

//XNOR GATE

subckt XNOR (VDD VSS A B out)

parameters wp=90n wn=90n ln=50n lp=50n mult=1

M0 (out A net0 VSS) NMOS\_VTL w=wn\*2 l=lp as=100n\*wn\*2 ad=100n\*wn\*2 ps=200n+wn\*2 pd=200n+wn\*2 m=mult

M1 (net0 net4 VSS VSS) NMOS\_VTL w=wn\*2 l=lp as=100n\*wn\*2 ad=100n\*wn\*2 ps=200n+wn\*2 pd=200n+wn\*2 m=mult

M2 (out B net1 VSS) NMOS\_VTL w=wn\*2 l=lp as=100n\*wn\*2 ad=100n\*wn\*2 ps=200n+wn\*2 pd=200n+wn\*2 m=mult

M3 (net1 net3 VSS VSS) NMOS\_VTL w=wn\*2 l=lp as=100n\*wn\*2 ad=100n\*wn\*2 ps=200n+wn\*2 pd=200n+wn\*2 m=mult

M4 (net2 B VDD VDD) PMOS\_VTL w=wp\*2 l=lp as=100n\*wp\*2 ad=100n\*wp\*2 ps=200n+wp\*2 pd=200n+wp\*2 m=mult

M5 (out net4 net2 VDD) PMOS\_VTL w=wp\*2 l=lp as=100n\*wp\*2 ad=100n\*wp\*2 ps=200n+wp\*2 pd=200n+wp\*2 m=mult

M6 (net2 net3 VDD VDD) PMOS\_VTL w=wp\*2 l=lp as=100n\*wp\*2 ad=100n\*wp\*2 ps=200n+wp\*2 pd=200n+wp\*2 m=mult

M7 (out A net2 VDD) PMOS\_VTL w=wp\*2 l=lp as=100n\*wp\*2 ad=100n\*wp\*2 ps=200n+wp\*2 pd=200n+wp\*2 m=mult

IA (VDD VSS A net3) Inverter

IB (VDD VSS B net4) Inverter

ends XNOR

//2:1 MUX 1bit

subckt mux1 (Cnt In1 In2 OUT VDD VSS)

M2 (net7 Cnt VSS VSS) NMOS\_VTL w=90n l=50n as=9.45e-15 ad=9.45e-15 ps=300n pd=300n ld=105n ls=105n m=1

M1 (In2 Cnt OUT VSS) NMOS\_VTL w=90n l=50n as=9.45e-15 ad=9.45e-15 ps=300n pd=300n ld=105n ls=105n m=1

M0 (In1 net7 OUT VSS) NMOS\_VTL w=90n l=50n as=9.45e-15 ad=9.45e-15 ps=300n pd=300n ld=105n ls=105n m=1

M5 (net7 Cnt VDD VDD) PMOS\_VTL w=90n l=50n as=9.45e-15 ad=9.45e-15 ps=300n pd=300n ld=105n ls=105n m=1

M4 (In2 net7 OUT VDD) PMOS\_VTL w=90n l=50n as=9.45e-15 ad=9.45e-15 ps=300n pd=300n ld=105n ls=105n m=1

M3 (In1 Cnt OUT VDD) PMOS\_VTL w=90n l=50n as=9.45e-15 ad=9.45e-15 ps=300n pd=300n ld=105n ls=105n m=1

ends mux1

//shifter

subckt shifter (Cntl1 Cntl2 VSS VDD In1 In2 In3 In4 In5 In6 In7 In8 In9 In10 In11 In12 In13 In14 In15 In16 Out1 Out2 Out3 Out4 Out5 Out6 Out7 Out8 Out9 Out10 Out11 Out12 Out13 Out14 Out15 Out16)

I1\_1 (Cntl1 VSS In1 out1\_1 VDD VSS) mux1

I1\_2 (Cntl1 In1 In2 out1\_2 VDD VSS) mux1

I1\_3 (Cntl1 In2 In3 out1\_3 VDD VSS) mux1

I1\_4 (Cntl1 In3 In4 out1\_4 VDD VSS) mux1

I1\_5 (Cntl1 In4 In5 out1\_5 VDD VSS) mux1

I1\_6 (Cntl1 In5 In6 out1\_6 VDD VSS) mux1

I1\_7 (Cntl1 In6 In7 out1\_7 VDD VSS) mux1

I1\_8 (Cntl1 In7 In8 out1\_8 VDD VSS) mux1

I1\_9 (Cntl1 In8 In9 out1\_9 VDD VSS) mux1

I1\_10 (Cntl1 In9 In10 out1\_10 VDD VSS) mux1

I1\_11 (Cntl1 In10 In11 out1\_11 VDD VSS) mux1

I1\_12 (Cntl1 In11 In12 out1\_12 VDD VSS) mux1

I1\_13 (Cntl1 In12 In13 out1\_13 VDD VSS) mux1

I1\_14 (Cntl1 In13 In14 out1\_14 VDD VSS) mux1

I1\_15 (Cntl1 In14 In15 out1\_15 VDD VSS) mux1

I1\_16 (Cntl1 In15 In16 out1\_16 VDD VSS) mux1

I2\_1 (cntmux2 VSS out1\_1 out2\_1 VDD VSS) mux1

I2\_2 (cntmux2 VSS out1\_2 out2\_2 VDD VSS) mux1

I2\_3 (cntmux2 out1\_1 out1\_3 out2\_3 VDD VSS) mux1

I2\_4 (cntmux2 out1\_2 out1\_4 out2\_4 VDD VSS) mux1

I2\_5 (cntmux2 out1\_3 out1\_5 out2\_5 VDD VSS) mux1

I2\_6 (cntmux2 out1\_4 out1\_6 out2\_6 VDD VSS) mux1

I2\_7 (cntmux2 out1\_5 out1\_7 out2\_7 VDD VSS) mux1

I2\_8 (cntmux2 out1\_6 out1\_8 out2\_8 VDD VSS) mux1

I2\_9 (cntmux2 out1\_7 out1\_9 out2\_9 VDD VSS) mux1

I2\_10 (cntmux2 out1\_8 out1\_10 out2\_10 VDD VSS) mux1

I2\_11 (cntmux2 out1\_9 out1\_11 out2\_11 VDD VSS) mux1

I2\_12 (cntmux2 out1\_10 out1\_12 out2\_12 VDD VSS) mux1

I2\_13 (cntmux2 out1\_11 out1\_13 out2\_13 VDD VSS) mux1

I2\_14 (cntmux2 out1\_12 out1\_14 out2\_14 VDD VSS) mux1

I2\_15 (cntmux2 out1\_13 out1\_15 out2\_15 VDD VSS) mux1

I2\_16 (cntmux2 out1\_14 out1\_16 out2\_16 VDD VSS) mux1

I3\_1 (cntmux3 VSS out2\_1 Out1 VDD VSS) mux1

I3\_2 (cntmux3 VSS out2\_2 Out2 VDD VSS) mux1

I3\_3 (cntmux3 VSS out2\_3 Out3 VDD VSS) mux1

I3\_4 (cntmux3 VSS out2\_4 Out4 VDD VSS) mux1

I3\_5 (cntmux3 out2\_1 out2\_5 Out5 VDD VSS) mux1

I3\_6 (cntmux3 out2\_2 out2\_6 Out6 VDD VSS) mux1

I3\_7 (cntmux3 out2\_3 out2\_7 Out7 VDD VSS) mux1

I3\_8 (cntmux3 out2\_4 out2\_8 Out8 VDD VSS) mux1

I3\_9 (cntmux3 out2\_5 out2\_9 Out9 VDD VSS) mux1

I3\_10 (cntmux3 out2\_6 out2\_10 Out10 VDD VSS) mux1

I3\_11 (cntmux3 out2\_7 out2\_11 Out11 VDD VSS) mux1

I3\_12 (cntmux3 out2\_8 out2\_12 Out12 VDD VSS) mux1

I3\_13 (cntmux3 out2\_9 out2\_13 Out13 VDD VSS) mux1

I3\_14 (cntmux3 out2\_10 out2\_14 Out14 VDD VSS) mux1

I3\_15 (cntmux3 out2\_11 out2\_15 Out15 VDD VSS) mux1

I3\_16 (cntmux3 out2\_12 out2\_16 Out16 VDD VSS) mux1

xnor1 (VDD VSS Cntl1 Cntl2 cntmux2) XNOR

nand1 (VDD VSS Cntl1 Cntl2 cntmux3) NAND

ends shifter

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*Mux\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

// Library name: Project

// Cell name: ece3663AND\_4in

// View name: schematic

subckt ece3663AND\_4in A B C D VDD VSS out

parameters wp=90n wn=90n ln=50n lp=50n mult=1

MN3 (net032 D VSS VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 ad=9.45e-15 ps=300n pd=300n m=1

MN0 (net053 A net033 VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 ad=9.45e-15 ps=300n pd=300n m=1

MN2 (neta C net032 VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 ad=9.45e-15 ps=300n pd=300n m=1

MN1 (net033 B neta VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 ad=9.45e-15 ps=300n pd=300n m=1

MP0 (net053 A VDD VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 ad=9.45e-15 ps=300n pd=300n m=1

MP3 (net053 D VDD VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 ad=9.45e-15 ps=300n pd=300n m=1

MP2 (net053 C VDD VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 ad=9.45e-15 ps=300n pd=300n m=1

MP1 (net053 B VDD VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 ad=9.45e-15 ps=300n pd=300n m=1

I1 (VDD VSS net053 out) ece3663Inverter\_1b

ends ece3663AND\_4in

// End of subcircuit definition.

// Library name: Project

// Cell name: ece3663OR\_8in

// View name: schematic

subckt ece3663OR\_8in I0 I1 I2 I3 I4 I5 I6 I7 VDD VSS out

parameters wp=90n wn=90n ln=50n lp=50n mult=1

M7 (net37 I7 VSS VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 ad=9.45e-15 ps=300n pd=300n m=1

M6 (net37 I6 VSS VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 ad=9.45e-15 ps=300n pd=300n m=1

M5 (net37 I5 VSS VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 ad=9.45e-15 ps=300n pd=300n m=1

M4 (net37 I4 VSS VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 ad=9.45e-15 ps=300n pd=300n m=1

M3 (net37 I3 VSS VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 ad=9.45e-15 ps=300n pd=300n m=1

M2 (net37 I2 VSS VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 ad=9.45e-15 ps=300n pd=300n m=1

M1 (net37 I1 VSS VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 ad=9.45e-15 ps=300n pd=300n m=1

M0 (net37 I0 VSS VSS) NMOS\_VTL w=wn l=ln as=9.45e-15 ad=9.45e-15 ps=300n pd=300n m=1

M15 (net48 I7 VDD VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 ad=9.45e-15 ps=300n pd=300n m=1

M14 (net52 I6 net48 VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 ad=9.45e-15 ps=300n pd=300n m=1

M13 (net56 I5 net52 VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 ad=9.45e-15 ps=300n pd=300n m=1

M12 (net60 I4 net56 VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 ad=9.45e-15 ps=300n pd=300n m=1

M11 (net64 I3 net60 VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 ad=9.45e-15 ps=300n pd=300n m=1

M10 (net68 I2 net64 VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 ad=9.45e-15 ps=300n pd=300n m=1

M9 (net72 I1 net68 VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 ad=9.45e-15 ps=300n pd=300n m=1

M8 (net37 I0 net72 VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 ad=9.45e-15 ps=300n pd=300n m=1

inverter (VDD VSS net37 out) ece3663Inverter\_1b

ends ece3663OR\_8in

// End of subcircuit definition.

// Library name: Project

// Cell name: ece3663MUX\_8-1

// View name: schematic

subckt mux I0 I1 I2 I3 I4 I5 I6 I7 VDD VSS out s0 s1 s2

parameters wp=90n wn=90n ln=50n lp=50n mult=1

AND7 (I7 s2 s1 s0 VDD VSS net3) ece3663AND\_4in

AND6 (I6 s2 s1 net7 VDD VSS net10) ece3663AND\_4in

AND5 (I5 s2 net27 s0 VDD VSS net17) ece3663AND\_4in

AND4 (I4 s2 net27 net7 VDD VSS net24) ece3663AND\_4in

AND3 (I3 net5 s1 s0 VDD VSS net31) ece3663AND\_4in

AND2 (I2 net5 s1 net7 VDD VSS net38) ece3663AND\_4in

AND1 (I1 net5 net27 s0 VDD VSS net45) ece3663AND\_4in

AND0 (I0 net5 net27 net7 VDD VSS net52) ece3663AND\_4in

I8 (net52 net45 net38 net31 net24 net17 net10 net3 VDD VSS out) ece3663OR\_8in

I11 (VDD VSS s2 net5) ece3663Inverter\_1b

I10 (VDD VSS s1 net27) ece3663Inverter\_1b

I9 (VDD VSS s0 net7) ece3663Inverter\_1b

ends mux

// End of subcircuit definition.

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*Register\_16b\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

subckt ece3663NOT VDD VSS in out

parameters mult=1

M0 (out in VSS VSS) NMOS\_VTL w=90n l=50n as=9.45e-15 ad=9.45e-15 ps=300n pd=300n ld=105n ls=105n m=mult

M1 (out in VDD VDD) PMOS\_VTL w=180.0n l=50n as=1.89e-14 ad=1.89e-14 ps=390.0n pd=390.0n ld=105n ls=105n m=mult

ends ece3663NOT

// End of subcircuit definition.

subckt ece3663Latch CLK CLKNOT D Q VDD VSS

M9 (VDD Q net11 VDD) PMOS\_VTL w=180.0n l=50n as=1.89e-14 ad=1.89e-14 ps=390.0n pd=390.0n ld=105n ls=105n m=1

M8 (net11 Q VSS VSS) NMOS\_VTL w=90n l=50n as=9.45e-15 ad=9.45e-15 ps=300n pd=300n ld=105n ls=105n m=1

M7 (Q CLKNOT net19 VSS) NMOS\_VTL w=180.0n l=50n as=1.89e-14 ad=1.89e-14 ps=390.0n pd=390.0n ld=105n ls=105n m=1

M6 (net19 net11 VSS VSS) NMOS\_VTL w=180.0n l=50n as=1.89e-14 ad=1.89e-14 ps=390.0n pd=390.0n ld=105n ls=105n m=1

M5 (net23 CLK Q VDD) PMOS\_VTL w=360.0n l=50n as=3.78e-14 ad=3.78e-14 ps=570.0n pd=570.0n ld=105n ls=105n m=1

M4 (VDD net11 net23 VDD) PMOS\_VTL w=360.0n l=50n as=3.78e-14 ad=3.78e-14 ps=570.0n pd=570.0n ld=105n ls=105n m=1

M3 (VDD D net35 VDD) PMOS\_VTL w=360.0n l=50n as=3.78e-14 ad=3.78e-14 ps=570.0n pd=570.0n ld=105n ls=105n m=1

M2 (net35 CLKNOT Q VDD) PMOS\_VTL w=360.0n l=50n as=3.78e-14 ad=3.78e-14 ps=570.0n pd=570.0n ld=105n ls=105n m=1

M1 (net39 D VSS VSS) NMOS\_VTL w=180.0n l=50n as=1.89e-14 ad=1.89e-14 ps=390.0n pd=390.0n ld=105n ls=105n m=1

M0 (Q CLK net39 VSS) NMOS\_VTL w=180.0n l=50n as=1.89e-14 ad=1.89e-14 ps=390.0n pd=390.0n ld=105n ls=105n m=1

ends ece3663Latch

// End of subcircuit definition.

subckt ece3663Register CLK D Q VDD VSS

I5 (VDD VSS CLK net106) ece3663NOT mult=1

I6 (net106 CLK D net118 VDD VSS) ece3663Latch

I4 (CLK net106 net118 Q VDD VSS) ece3663Latch

ends ece3663Register

// Library name: Project

// Cell name: ece3663Register\_16b

// View name: schematic

subckt ece3663Register\_16b VDD VSS CLK D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15 Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8 Q9 Q10 Q11 Q12 Q13 Q14 Q15

I0\<0\> (CLK D0 Q0 VDD VSS) ece3663Register

I0\<1\> (CLK D1 Q1 VDD VSS) ece3663Register

I0\<2\> (CLK D2 Q2 VDD VSS) ece3663Register

I0\<3\> (CLK D3 Q3 VDD VSS) ece3663Register

I0\<4\> (CLK D4 Q4 VDD VSS) ece3663Register

I0\<5\> (CLK D5 Q5 VDD VSS) ece3663Register

I0\<6\> (CLK D6 Q6 VDD VSS) ece3663Register

I0\<7\> (CLK D7 Q7 VDD VSS) ece3663Register

I0\<8\> (CLK D8 Q8 VDD VSS) ece3663Register

I0\<9\> (CLK D9 Q9 VDD VSS) ece3663Register

I0\<10\> (CLK D10 Q10 VDD VSS) ece3663Register

I0\<11\> (CLK D11 Q11 VDD VSS) ece3663Register

I0\<12\> (CLK D12 Q12 VDD VSS) ece3663Register

I0\<13\> (CLK D13 Q13 VDD VSS) ece3663Register

I0\<14\> (CLK D14 Q14 VDD VSS) ece3663Register

I0\<15\> (CLK D15 Q15 VDD VSS) ece3663Register

ends ece3663Register\_16b

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*Wallace Tree Multiplier \*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

// Library name: Project

// Cell name: ece3663AND\_1b

// View name: schematic

subckt ece3663AND\_1b VDD VSS A B out

parameters wp=90n wn=90n ln=50n lp=50n mult=1

MN0 (net1 B VSS VSS) NMOS\_VTL w=2\*wn l=ln as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MN1 (net0 A net1 VSS) NMOS\_VTL w=2\*wn l=ln \

as=9.45e-15 ad=9.45e-15 ps=300n pd=300n m=1

MP0 (net0 A VDD VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

MP1 (net0 B VDD VDD) PMOS\_VTL w=wp l=lp as=9.45e-15 \

ad=9.45e-15 ps=300n pd=300n m=1

I0 (VDD VSS net0 out) ece3663Inverter\_1b

ends ece3663AND\_1b

// End of subcircuit definition.

// Library name: Project

// Cell name: ece3663mult\_ppgen

// View name: schematic

subckt ece3663mult\_ppgen VDD VSS A0 A1 A2 A3 A4 A5 A6 A7 B0 B1 B2 B3 B4 B5 B6 B7 \

pp\_0\_0 \

pp\_1\_0 pp\_0\_1 \

pp\_2\_0 pp\_1\_1 pp\_0\_2 \

pp\_3\_0 pp\_2\_1 pp\_1\_2 pp\_0\_3 \

pp\_4\_0 pp\_3\_1 pp\_2\_2 pp\_1\_3 pp\_0\_4 \

pp\_5\_0 pp\_4\_1 pp\_3\_2 pp\_2\_3 pp\_1\_4 pp\_0\_5 \

pp\_6\_0 pp\_5\_1 pp\_4\_2 pp\_3\_3 pp\_2\_4 pp\_1\_5 pp\_0\_6 \

pp\_7\_0 pp\_6\_1 pp\_5\_2 pp\_4\_3 pp\_3\_4 pp\_2\_5 pp\_1\_6 pp\_0\_7 \

pp\_7\_1 pp\_6\_2 pp\_5\_3 pp\_4\_4 pp\_3\_5 pp\_2\_6 pp\_1\_7 \

pp\_7\_2 pp\_6\_3 pp\_5\_4 pp\_4\_5 pp\_3\_6 pp\_2\_7 \

pp\_7\_3 pp\_6\_4 pp\_5\_5 pp\_4\_6 pp\_3\_7 \

pp\_7\_4 pp\_6\_5 pp\_5\_6 pp\_4\_7 \

pp\_7\_5 pp\_6\_6 pp\_5\_7 \

pp\_7\_6 pp\_6\_7 \

pp\_7\_7

A00 (VDD VSS A0 B0 pp\_0\_0) ece3663AND\_1b

A10 (VDD VSS A1 B0 pp\_1\_0) ece3663AND\_1b

A01 (VDD VSS A0 B1 pp\_0\_1) ece3663AND\_1b

A20 (VDD VSS A2 B0 pp\_2\_0) ece3663AND\_1b

A11 (VDD VSS A1 B1 pp\_1\_1) ece3663AND\_1b

A02 (VDD VSS A0 B2 pp\_0\_2) ece3663AND\_1b

A30 (VDD VSS A3 B0 pp\_3\_0) ece3663AND\_1b

A21 (VDD VSS A2 B1 pp\_2\_1) ece3663AND\_1b

A12 (VDD VSS A1 B2 pp\_1\_2) ece3663AND\_1b

A03 (VDD VSS A0 B3 pp\_0\_3) ece3663AND\_1b

A40 (VDD VSS A4 B0 pp\_4\_0) ece3663AND\_1b

A31 (VDD VSS A3 B1 pp\_3\_1) ece3663AND\_1b

A22 (VDD VSS A2 B2 pp\_2\_2) ece3663AND\_1b

A13 (VDD VSS A1 B3 pp\_1\_3) ece3663AND\_1b

A04 (VDD VSS A0 B4 pp\_0\_4) ece3663AND\_1b

A50 (VDD VSS A5 B0 pp\_5\_0) ece3663AND\_1b

A41 (VDD VSS A4 B1 pp\_4\_1) ece3663AND\_1b

A32 (VDD VSS A3 B2 pp\_3\_2) ece3663AND\_1b

A23 (VDD VSS A2 B3 pp\_2\_3) ece3663AND\_1b

A14 (VDD VSS A1 B4 pp\_1\_4) ece3663AND\_1b

A05 (VDD VSS A0 B5 pp\_0\_5) ece3663AND\_1b

A60 (VDD VSS A6 B0 pp\_6\_0) ece3663AND\_1b

A51 (VDD VSS A5 B1 pp\_5\_1) ece3663AND\_1b

A42 (VDD VSS A4 B2 pp\_4\_2) ece3663AND\_1b

A33 (VDD VSS A3 B3 pp\_3\_3) ece3663AND\_1b

A24 (VDD VSS A2 B4 pp\_2\_4) ece3663AND\_1b

A15 (VDD VSS A1 B5 pp\_1\_5) ece3663AND\_1b

A06 (VDD VSS A0 B6 pp\_0\_6) ece3663AND\_1b

A70 (VDD VSS A7 B0 pp\_7\_0) ece3663AND\_1b

A61 (VDD VSS A6 B1 pp\_6\_1) ece3663AND\_1b

A52 (VDD VSS A5 B2 pp\_5\_2) ece3663AND\_1b

A43 (VDD VSS A4 B3 pp\_4\_3) ece3663AND\_1b

A34 (VDD VSS A3 B4 pp\_3\_4) ece3663AND\_1b

A25 (VDD VSS A2 B5 pp\_2\_5) ece3663AND\_1b

A16 (VDD VSS A1 B6 pp\_1\_6) ece3663AND\_1b

A07 (VDD VSS A0 B7 pp\_0\_7) ece3663AND\_1b

A71 (VDD VSS A7 B1 pp\_7\_1) ece3663AND\_1b

A62 (VDD VSS A6 B2 pp\_6\_2) ece3663AND\_1b

A53 (VDD VSS A5 B3 pp\_5\_3) ece3663AND\_1b

A44 (VDD VSS A4 B4 pp\_4\_4) ece3663AND\_1b

A35 (VDD VSS A3 B5 pp\_3\_5) ece3663AND\_1b

A26 (VDD VSS A2 B6 pp\_2\_6) ece3663AND\_1b

A17 (VDD VSS A1 B7 pp\_1\_7) ece3663AND\_1b

A72 (VDD VSS A7 B2 pp\_7\_2) ece3663AND\_1b

A63 (VDD VSS A6 B3 pp\_6\_3) ece3663AND\_1b

A54 (VDD VSS A5 B4 pp\_5\_4) ece3663AND\_1b

A45 (VDD VSS A4 B5 pp\_4\_5) ece3663AND\_1b

A36 (VDD VSS A3 B6 pp\_3\_6) ece3663AND\_1b

A27 (VDD VSS A2 B7 pp\_2\_7) ece3663AND\_1b

A73 (VDD VSS A7 B3 pp\_7\_3) ece3663AND\_1b

A64 (VDD VSS A6 B4 pp\_6\_4) ece3663AND\_1b

A55 (VDD VSS A5 B5 pp\_5\_5) ece3663AND\_1b

A46 (VDD VSS A4 B6 pp\_4\_6) ece3663AND\_1b

A37 (VDD VSS A3 B7 pp\_3\_7) ece3663AND\_1b

A74 (VDD VSS A7 B4 pp\_7\_4) ece3663AND\_1b

A65 (VDD VSS A6 B5 pp\_6\_5) ece3663AND\_1b

A56 (VDD VSS A5 B6 pp\_5\_6) ece3663AND\_1b

A47 (VDD VSS A4 B7 pp\_4\_7) ece3663AND\_1b

A75 (VDD VSS A7 B5 pp\_7\_5) ece3663AND\_1b

A66 (VDD VSS A6 B6 pp\_6\_6) ece3663AND\_1b

A57 (VDD VSS A5 B7 pp\_5\_7) ece3663AND\_1b

A76 (VDD VSS A7 B6 pp\_7\_6) ece3663AND\_1b

A67 (VDD VSS A6 B7 pp\_6\_7) ece3663AND\_1b

A77 (VDD VSS A7 B7 pp\_7\_7) ece3663AND\_1b

ends ece3663mult\_ppgen

//

//unmirrored adder for wallace tree stages

// Library name: Project

// Cell name: Adder\_nm

// View name: schematic

subckt Adder\_nm A B Cin Cout Sum Vdd Vss

U0 (A B Cin net0 net1 Vdd Vss) Adder

I0 (Vdd Vss net0 Cout) ece3663Inverter\_1b

I1 (Vdd Vss net1 Sum) ece3663Inverter\_1b

ends Adder\_nm

//wallace tree stage 1

// Library name: Project

// Cell name: ece3663mult\_WT1

// View name: schematic

subckt ece3663mult\_WT1 VDD VSS \

pp\_1\_0 pp\_0\_1 \

pp\_2\_0 pp\_1\_1 pp\_0\_2 \

pp\_3\_0 pp\_2\_1 pp\_1\_2 \

pp\_4\_0 pp\_3\_1 pp\_2\_2 pp\_1\_3 pp\_0\_4 \

pp\_5\_0 pp\_4\_1 pp\_3\_2 pp\_2\_3 pp\_1\_4 pp\_0\_5\

pp\_6\_0 pp\_5\_1 pp\_4\_2 pp\_3\_3 pp\_2\_4 pp\_1\_5\

pp\_7\_0 pp\_6\_1 pp\_5\_2 pp\_4\_3 pp\_3\_4 pp\_2\_5\

pp\_7\_1 pp\_6\_2 pp\_5\_3 pp\_4\_4 pp\_3\_5 \

pp\_7\_2 pp\_6\_3 pp\_5\_4 \

pp\_7\_3 pp\_6\_4 pp\_5\_5 \

pp\_7\_4 pp\_6\_5 \

w1\_1\_0 \

w1\_2\_0 w1\_1\_1 \

w1\_3\_0 w1\_2\_1 \

w1\_4\_0 w1\_3\_1 w1\_2\_2 \

w1\_5\_0 w1\_4\_1 w1\_3\_2 w1\_2\_3 \

w1\_6\_0 w1\_5\_1 w1\_4\_2 w1\_3\_3 \

w1\_7\_0 w1\_6\_1 w1\_5\_2 w1\_4\_3 \

w1\_7\_1 w1\_6\_2 w1\_5\_3 w1\_4\_4 \

w1\_7\_2 w1\_6\_3 w1\_5\_4 \

w1\_7\_3 w1\_6\_4 \

w1\_7\_4 w1\_6\_5 \

w1\_7\_5

U10 (pp\_1\_0 pp\_0\_1 VSS w1\_2\_0 w1\_1\_0 VDD VSS) Adder\_nm

U20 (pp\_2\_0 pp\_1\_1 pp\_0\_2 w1\_3\_0 w1\_1\_1 VDD VSS) Adder\_nm

U30 (pp\_3\_0 pp\_2\_1 pp\_1\_2 w1\_4\_0 w1\_2\_1 VDD VSS) Adder\_nm

U40 (pp\_4\_0 pp\_3\_1 pp\_2\_2 w1\_5\_0 w1\_3\_1 VDD VSS) Adder\_nm

U13 (pp\_1\_3 pp\_0\_4 VSS w1\_4\_1 w1\_2\_2 VDD VSS) Adder\_nm

U50 (pp\_5\_0 pp\_4\_1 pp\_3\_2 w1\_6\_0 w1\_3\_2 VDD VSS) Adder\_nm

U23 (pp\_2\_3 pp\_1\_4 pp\_0\_5 w1\_5\_1 w1\_2\_3 VDD VSS) Adder\_nm

U60 (pp\_6\_0 pp\_5\_1 pp\_4\_2 w1\_7\_0 w1\_4\_2 VDD VSS) Adder\_nm

U33 (pp\_3\_3 pp\_2\_4 pp\_1\_5 w1\_6\_1 w1\_3\_3 VDD VSS) Adder\_nm

U70 (pp\_7\_0 pp\_6\_1 pp\_5\_2 w1\_7\_1 w1\_5\_2 VDD VSS) Adder\_nm

U43 (pp\_4\_3 pp\_3\_4 pp\_2\_5 w1\_6\_2 w1\_4\_3 VDD VSS) Adder\_nm

U71 (pp\_7\_1 pp\_6\_2 pp\_5\_3 w1\_7\_2 w1\_5\_3 VDD VSS) Adder\_nm

U44 (pp\_4\_4 pp\_3\_5 VSS w1\_6\_3 w1\_4\_4 VDD VSS) Adder\_nm

U72 (pp\_7\_2 pp\_6\_3 pp\_5\_4 w1\_7\_3 w1\_5\_4 VDD VSS) Adder\_nm

U73 (pp\_7\_3 pp\_6\_4 pp\_5\_5 w1\_7\_4 w1\_6\_4 VDD VSS) Adder\_nm

U74 (pp\_7\_4 pp\_6\_5 VSS w1\_7\_5 w1\_6\_5 VDD VSS) Adder\_nm

ends ece3663mult\_WT1

//wallace tree stage 2

// Library name: Project

// Cell name: ece3663mult\_WT2

// View name: schematic

subckt ece3663mult\_WT2 VDD VSS \

w1\_2\_0 w1\_1\_1 \

w1\_3\_0 w1\_2\_1 pp\_0\_3 \

w1\_4\_0 w1\_3\_1 w1\_2\_2 \

w1\_5\_0 w1\_4\_1 w1\_3\_2 \

w1\_6\_0 w1\_5\_1 w1\_4\_2 w1\_3\_3 pp\_0\_6 \

w1\_7\_0 w1\_6\_1 w1\_5\_2 w1\_4\_3 pp\_1\_6 pp\_0\_7 \

w1\_7\_1 w1\_6\_2 w1\_5\_3 w1\_4\_4 pp\_2\_6 pp\_1\_7 \

w1\_7\_2 w1\_6\_3 w1\_5\_4 pp\_4\_5 pp\_3\_6 pp\_2\_7 \

w1\_7\_3 w1\_6\_4 pp\_4\_6 \

w1\_7\_4 w1\_6\_5 pp\_5\_6 \

w1\_7\_5 pp\_7\_5 pp\_6\_6 \

pp\_7\_6 pp\_6\_7 \

w2\_2\_0 \

w2\_3\_0 w2\_2\_1 \

w2\_4\_0 w2\_3\_1 \

w2\_5\_0 w2\_4\_1 \

w2\_6\_0 w2\_5\_1 w2\_4\_2 \

w2\_7\_0 w2\_6\_1 w2\_5\_2 w2\_4\_3 \

w2\_7\_1 w2\_6\_2 w2\_5\_3 w2\_4\_4 \

w2\_7\_2 w2\_6\_3 w2\_5\_4 w2\_4\_5 \

w2\_7\_3 w2\_6\_4 w2\_5\_5 \

w2\_7\_4 w2\_6\_5 \

w2\_7\_5 w2\_6\_6 \

w2\_7\_6 w2\_6\_7 \

w2\_7\_7

U20 (w1\_2\_0 w1\_1\_1 VSS w2\_3\_0 w2\_2\_0 VDD VSS) Adder\_nm

U30 (w1\_3\_0 w1\_2\_1 pp\_0\_3 w2\_4\_0 w2\_2\_1 VDD VSS) Adder\_nm

U40 (w1\_4\_0 w1\_3\_1 w1\_2\_2 w2\_5\_0 w2\_3\_1 VDD VSS) Adder\_nm

U50 (w1\_5\_0 w1\_4\_1 w1\_3\_2 w2\_6\_0 w2\_4\_1 VDD VSS) Adder\_nm

U60 (w1\_6\_0 w1\_5\_1 w1\_4\_2 w2\_7\_0 w2\_5\_1 VDD VSS) Adder\_nm

U33 (w1\_3\_3 pp\_0\_6 VSS w2\_6\_1 w2\_4\_2 VDD VSS) Adder\_nm

U70 (w1\_7\_0 w1\_6\_1 w1\_5\_2 w2\_7\_1 w2\_5\_2 VDD VSS) Adder\_nm

U43 (w1\_4\_3 pp\_1\_6 pp\_0\_7 w2\_6\_2 w2\_4\_3 VDD VSS) Adder\_nm

U71 (w1\_7\_1 w1\_6\_2 w1\_5\_3 w2\_7\_2 w2\_5\_3 VDD VSS) Adder\_nm

U44 (w1\_4\_4 pp\_2\_6 pp\_1\_7 w2\_6\_3 w2\_4\_4 VDD VSS) Adder\_nm

U72 (w1\_7\_2 w1\_6\_3 w1\_5\_4 w2\_7\_3 w2\_5\_4 VDD VSS) Adder\_nm

U45 (pp\_4\_5 pp\_3\_6 pp\_2\_7 w2\_6\_4 w2\_4\_5 VDD VSS) Adder\_nm

U73 (w1\_7\_3 w1\_6\_4 pp\_4\_6 w2\_7\_4 w2\_5\_5 VDD VSS) Adder\_nm

U74 (w1\_7\_4 w1\_6\_5 pp\_5\_6 w2\_7\_5 w2\_6\_5 VDD VSS) Adder\_nm

U75 (w1\_7\_5 pp\_7\_5 pp\_6\_6 w2\_7\_6 w2\_6\_6 VDD VSS) Adder\_nm

U76 (pp\_7\_6 pp\_6\_7 VSS w2\_7\_7 w2\_6\_7 VDD VSS) Adder\_nm

ends ece3663mult\_WT2

//wallace tree stage 3

// Library name: Project

// Cell name: ece3663mult\_WT3

// View name: schematic

subckt ece3663mult\_WT3 VDD VSS \

w2\_3\_0 w2\_2\_1 \

w2\_4\_0 w2\_3\_1 \

w2\_5\_0 w2\_4\_1 w1\_2\_3 \

w2\_6\_0 w2\_5\_1 w2\_4\_2 \

w2\_7\_0 w2\_6\_1 w2\_5\_2 \

w2\_7\_1 w2\_6\_2 w2\_5\_3 \

w2\_7\_2 w2\_6\_3 w2\_5\_4 \

w2\_7\_3 w2\_6\_4 w2\_5\_5 \

w2\_7\_4 w2\_6\_5 \

w2\_7\_5 w2\_6\_6 \

w3\_3\_0 \

w3\_4\_0 w3\_3\_1 \

w3\_5\_0 w3\_4\_1 \

w3\_6\_0 w3\_5\_1 \

w3\_7\_0 w3\_6\_1 \

w3\_7\_1 w3\_6\_2 \

w3\_7\_2 w3\_6\_3 \

w3\_7\_3 w3\_6\_4 \

w3\_7\_4 w3\_6\_5 \

w3\_7\_5 w3\_6\_6 \

w3\_7\_6

U30 (w2\_3\_0 w2\_2\_1 VSS w3\_4\_0 w3\_3\_0 VDD VSS) Adder\_nm

U40 (w2\_4\_0 w2\_3\_1 VSS w3\_5\_0 w3\_3\_1 VDD VSS) Adder\_nm

U50 (w2\_5\_0 w2\_4\_1 w1\_2\_3 w3\_6\_0 w3\_4\_1 VDD VSS) Adder\_nm

U60 (w2\_6\_0 w2\_5\_1 w2\_4\_2 w3\_7\_0 w3\_5\_1 VDD VSS) Adder\_nm

U70 (w2\_7\_0 w2\_6\_1 w2\_5\_2 w3\_7\_1 w3\_6\_1 VDD VSS) Adder\_nm

U71 (w2\_7\_1 w2\_6\_2 w2\_5\_3 w3\_7\_2 w3\_6\_2 VDD VSS) Adder\_nm

U72 (w2\_7\_2 w2\_6\_3 w2\_5\_4 w3\_7\_3 w3\_6\_3 VDD VSS) Adder\_nm

U73 (w2\_7\_3 w2\_6\_4 w2\_5\_5 w3\_7\_4 w3\_6\_4 VDD VSS) Adder\_nm

U74 (w2\_7\_4 w2\_6\_5 VSS w3\_7\_5 w3\_6\_5 VDD VSS) Adder\_nm

U75 (w2\_7\_5 w2\_6\_6 VSS w3\_7\_6 w3\_6\_6 VDD VSS) Adder\_nm

ends ece3663mult\_WT3

//wallace tree stage 4

// Library name: Project

// Cell name: ece3663mult\_WT4

// View name: schematic

subckt ece3663mult\_WT4 VDD VSS \

w3\_4\_0 w3\_3\_1 \

w3\_5\_0 w3\_4\_1 \

w3\_6\_0 w3\_5\_1 \

w3\_7\_0 w3\_6\_1 w2\_4\_3 \

w3\_7\_1 w3\_6\_2 w2\_4\_4 \

w3\_7\_2 w3\_6\_3 w2\_4\_5 \

w3\_7\_3 w3\_6\_4 pp\_3\_7 \

w3\_7\_4 w3\_6\_5 pp\_4\_7 \

w3\_7\_5 w3\_6\_6 pp\_5\_7 \

w3\_7\_6 w2\_7\_6 w2\_6\_7 \

w2\_7\_7 pp\_7\_7 \

w4\_4\_0 \

w4\_5\_0 w4\_4\_1 \

w4\_6\_0 w4\_5\_1 \

w4\_7\_0 w4\_6\_1 \

w4\_7\_1 w4\_6\_2 \

w4\_7\_2 w4\_6\_3 \

w4\_7\_3 w4\_6\_4 \

w4\_7\_4 w4\_6\_5 \

w4\_7\_5 w4\_6\_6 \

w4\_7\_6 w4\_6\_7 \

w4\_7\_7 w4\_6\_8 \

w4\_7\_8

U40 (w3\_4\_0 w3\_3\_1 VSS w4\_5\_0 w4\_4\_0 VDD VSS) Adder\_nm

U50 (w3\_5\_0 w3\_4\_1 VSS w4\_6\_0 w4\_4\_1 VDD VSS) Adder\_nm

U60 (w3\_6\_0 w3\_5\_1 VSS w4\_7\_0 w4\_5\_1 VDD VSS) Adder\_nm

U70 (w3\_7\_0 w3\_6\_1 w2\_4\_3 w4\_7\_1 w4\_6\_1 VDD VSS) Adder\_nm

U71 (w3\_7\_1 w3\_6\_2 w2\_4\_4 w4\_7\_2 w4\_6\_2 VDD VSS) Adder\_nm

U72 (w3\_7\_2 w3\_6\_3 w2\_4\_5 w4\_7\_3 w4\_6\_3 VDD VSS) Adder\_nm

U73 (w3\_7\_3 w3\_6\_4 pp\_3\_7 w4\_7\_4 w4\_6\_4 VDD VSS) Adder\_nm

U74 (w3\_7\_4 w3\_6\_5 pp\_4\_7 w4\_7\_5 w4\_6\_5 VDD VSS) Adder\_nm

U75 (w3\_7\_5 w3\_6\_6 pp\_5\_7 w4\_7\_6 w4\_6\_6 VDD VSS) Adder\_nm

U76 (w3\_7\_6 w2\_7\_6 w2\_6\_7 w4\_7\_7 w4\_6\_7 VDD VSS) Adder\_nm

U77 (w2\_7\_7 pp\_7\_7 VSS w4\_7\_8 w4\_6\_8 VDD VSS) Adder\_nm

ends ece3663mult\_WT4

//fast adder

// Library name: Project

// Cell name: ece3663mult\_FA

// View name: schematic

subckt ece3663mult\_FA VDD VSS w4\_5\_0 w4\_4\_1 w4\_6\_0 w4\_5\_1 w4\_7\_0 w4\_6\_1 \

w4\_7\_1 w4\_6\_2 w4\_7\_2 w4\_6\_3 w4\_7\_3 w4\_6\_4 w4\_7\_4 w4\_6\_5 w4\_7\_5 \

w4\_6\_6 w4\_7\_6 w4\_6\_7 w4\_7\_7 w4\_6\_8 w4\_7\_8 \

OUT5 OUT6 OUT7 OUT8 OUT9 OUT10 OUT11 OUT12 OUT13 OUT14 OUT15 Cout

U5 (w4\_5\_0 w4\_4\_1 VSS C0 net5 VDD VSS) Adder

I5 (VDD VSS net5 OUT5) ece3663Inverter\_1b

I60 (VDD VSS w4\_6\_0 net60) ece3663Inverter\_1b

I51 (VDD VSS w4\_5\_1 net51) ece3663Inverter\_1b

U6 (net60 net51 C0 C1 OUT6 VDD VSS) Adder

U7 (w4\_7\_0 w4\_6\_1 C1 C2 net7 VDD VSS) Adder

I7 (VDD VSS net7 OUT7) ece3663Inverter\_1b

I62 (VDD VSS w4\_6\_2 net62) ece3663Inverter\_1b

I71 (VDD VSS w4\_7\_1 net71) ece3663Inverter\_1b

U8 (net62 net71 C2 C3 OUT8 VDD VSS) Adder

U9 (w4\_7\_2 w4\_6\_3 C3 C4 net9 VDD VSS) Adder

I9 (VDD VSS net9 OUT9) ece3663Inverter\_1b

I64 (VDD VSS w4\_6\_4 net64) ece3663Inverter\_1b

I73 (VDD VSS w4\_7\_3 net73) ece3663Inverter\_1b

U10 (net64 net73 C4 C5 OUT10 VDD VSS) Adder

U11 (w4\_7\_4 w4\_6\_5 C5 C6 net11 VDD VSS) Adder

I11 (VDD VSS net11 OUT11) ece3663Inverter\_1b

I66 (VDD VSS w4\_6\_6 net66) ece3663Inverter\_1b

I75 (VDD VSS w4\_7\_5 net75) ece3663Inverter\_1b

U12 (net66 net75 C6 C7 OUT12 VDD VSS) Adder

U13 (w4\_7\_6 w4\_6\_7 C7 C8 net13 VDD VSS) Adder

I13 (VDD VSS net13 OUT13) ece3663Inverter\_1b

I68 (VDD VSS w4\_6\_8 net68) ece3663Inverter\_1b

I77 (VDD VSS w4\_7\_7 net77) ece3663Inverter\_1b

U14 (net68 net77 C8 C9 OUT14 VDD VSS) Adder

U15 (w4\_7\_8 VSS C9 Cinv net15 VDD VSS) Adder

I15 (VDD VSS net15 OUT15) ece3663Inverter\_1b

I16 (VDD VSS Cinv Cout) ece3663Inverter\_1b

ends ece3663mult\_FA

//multiplier subcircuit

// Library name: Project

// Cell name: ece3663multiplier

// View name: schematic

subckt ece3663multiplier VDD VSS A0 A1 A2 A3 A4 A5 A6 A7 B0 B1 B2 B3 B4 B5 B6 B7 \

Cout OUT0 OUT1 OUT2 OUT3 OUT4 OUT5 OUT6 OUT7 OUT8 OUT9 OUT10 OUT11 OUT12 OUT13 OUT14 OUT15

P0 (VDD VSS A0 A1 A2 A3 A4 A5 A6 A7 B0 B1 B2 B3 B4 B5 B6 B7 \

OUT0 \

pp\_1\_0 pp\_0\_1 \

pp\_2\_0 pp\_1\_1 pp\_0\_2 \

pp\_3\_0 pp\_2\_1 pp\_1\_2 pp\_0\_3 \

pp\_4\_0 pp\_3\_1 pp\_2\_2 pp\_1\_3 pp\_0\_4 \

pp\_5\_0 pp\_4\_1 pp\_3\_2 pp\_2\_3 pp\_1\_4 pp\_0\_5 \

pp\_6\_0 pp\_5\_1 pp\_4\_2 pp\_3\_3 pp\_2\_4 pp\_1\_5 pp\_0\_6 \

pp\_7\_0 pp\_6\_1 pp\_5\_2 pp\_4\_3 pp\_3\_4 pp\_2\_5 pp\_1\_6 pp\_0\_7 \

pp\_7\_1 pp\_6\_2 pp\_5\_3 pp\_4\_4 pp\_3\_5 pp\_2\_6 pp\_1\_7 \

pp\_7\_2 pp\_6\_3 pp\_5\_4 pp\_4\_5 pp\_3\_6 pp\_2\_7 \

pp\_7\_3 pp\_6\_4 pp\_5\_5 pp\_4\_6 pp\_3\_7 \

pp\_7\_4 pp\_6\_5 pp\_5\_6 pp\_4\_7 \

pp\_7\_5 pp\_6\_6 pp\_5\_7 \

pp\_7\_6 pp\_6\_7 \

pp\_7\_7) ece3663mult\_ppgen

W1 (VDD VSS \

pp\_1\_0 pp\_0\_1 \

pp\_2\_0 pp\_1\_1 pp\_0\_2 \

pp\_3\_0 pp\_2\_1 pp\_1\_2 \

pp\_4\_0 pp\_3\_1 pp\_2\_2 pp\_1\_3 pp\_0\_4 \

pp\_5\_0 pp\_4\_1 pp\_3\_2 pp\_2\_3 pp\_1\_4 pp\_0\_5\

pp\_6\_0 pp\_5\_1 pp\_4\_2 pp\_3\_3 pp\_2\_4 pp\_1\_5\

pp\_7\_0 pp\_6\_1 pp\_5\_2 pp\_4\_3 pp\_3\_4 pp\_2\_5\

pp\_7\_1 pp\_6\_2 pp\_5\_3 pp\_4\_4 pp\_3\_5 \

pp\_7\_2 pp\_6\_3 pp\_5\_4 \

pp\_7\_3 pp\_6\_4 pp\_5\_5 \

pp\_7\_4 pp\_6\_5 \

OUT1 \

w1\_2\_0 w1\_1\_1 \

w1\_3\_0 w1\_2\_1 \

w1\_4\_0 w1\_3\_1 w1\_2\_2 \

w1\_5\_0 w1\_4\_1 w1\_3\_2 w1\_2\_3 \

w1\_6\_0 w1\_5\_1 w1\_4\_2 w1\_3\_3 \

w1\_7\_0 w1\_6\_1 w1\_5\_2 w1\_4\_3 \

w1\_7\_1 w1\_6\_2 w1\_5\_3 w1\_4\_4 \

w1\_7\_2 w1\_6\_3 w1\_5\_4 \

w1\_7\_3 w1\_6\_4 \

w1\_7\_4 w1\_6\_5 \

w1\_7\_5) ece3663mult\_WT1

W2 (VDD VSS \

w1\_2\_0 w1\_1\_1 \

w1\_3\_0 w1\_2\_1 pp\_0\_3 \

w1\_4\_0 w1\_3\_1 w1\_2\_2 \

w1\_5\_0 w1\_4\_1 w1\_3\_2 \

w1\_6\_0 w1\_5\_1 w1\_4\_2 w1\_3\_3 pp\_0\_6 \

w1\_7\_0 w1\_6\_1 w1\_5\_2 w1\_4\_3 pp\_1\_6 pp\_0\_7 \

w1\_7\_1 w1\_6\_2 w1\_5\_3 w1\_4\_4 pp\_2\_6 pp\_1\_7 \

w1\_7\_2 w1\_6\_3 w1\_5\_4 pp\_4\_5 pp\_3\_6 pp\_2\_7 \

w1\_7\_3 w1\_6\_4 pp\_4\_6 \

w1\_7\_4 w1\_6\_5 pp\_5\_6 \

w1\_7\_5 pp\_7\_5 pp\_6\_6 \

pp\_7\_6 pp\_6\_7 \

OUT2 \

w2\_3\_0 w2\_2\_1 \

w2\_4\_0 w2\_3\_1 \

w2\_5\_0 w2\_4\_1 \

w2\_6\_0 w2\_5\_1 w2\_4\_2 \

w2\_7\_0 w2\_6\_1 w2\_5\_2 w2\_4\_3 \

w2\_7\_1 w2\_6\_2 w2\_5\_3 w2\_4\_4 \

w2\_7\_2 w2\_6\_3 w2\_5\_4 w2\_4\_5 \

w2\_7\_3 w2\_6\_4 w2\_5\_5 \

w2\_7\_4 w2\_6\_5 \

w2\_7\_5 w2\_6\_6 \

w2\_7\_6 w2\_6\_7 \

w2\_7\_7) ece3663mult\_WT2

W3 (VDD VSS \

w2\_3\_0 w2\_2\_1 \

w2\_4\_0 w2\_3\_1 \

w2\_5\_0 w2\_4\_1 w1\_2\_3 \

w2\_6\_0 w2\_5\_1 w2\_4\_2 \

w2\_7\_0 w2\_6\_1 w2\_5\_2 \

w2\_7\_1 w2\_6\_2 w2\_5\_3 \

w2\_7\_2 w2\_6\_3 w2\_5\_4 \

w2\_7\_3 w2\_6\_4 w2\_5\_5 \

w2\_7\_4 w2\_6\_5 \

w2\_7\_5 w2\_6\_6 \

OUT3 \

w3\_4\_0 w3\_3\_1 \

w3\_5\_0 w3\_4\_1 \

w3\_6\_0 w3\_5\_1 \

w3\_7\_0 w3\_6\_1 \

w3\_7\_1 w3\_6\_2 \

w3\_7\_2 w3\_6\_3 \

w3\_7\_3 w3\_6\_4 \

w3\_7\_4 w3\_6\_5 \

w3\_7\_5 w3\_6\_6 \

w3\_7\_6) ece3663mult\_WT3

W4 (VDD VSS \

w3\_4\_0 w3\_3\_1 \

w3\_5\_0 w3\_4\_1 \

w3\_6\_0 w3\_5\_1 \

w3\_7\_0 w3\_6\_1 w2\_4\_3 \

w3\_7\_1 w3\_6\_2 w2\_4\_4 \

w3\_7\_2 w3\_6\_3 w2\_4\_5 \

w3\_7\_3 w3\_6\_4 pp\_3\_7 \

w3\_7\_4 w3\_6\_5 pp\_4\_7 \

w3\_7\_5 w3\_6\_6 pp\_5\_7 \

w3\_7\_6 w2\_7\_6 w2\_6\_7 \

w2\_7\_7 pp\_7\_7 \

OUT4 \

w4\_5\_0 w4\_4\_1 \

w4\_6\_0 w4\_5\_1 \

w4\_7\_0 w4\_6\_1 \

w4\_7\_1 w4\_6\_2 \

w4\_7\_2 w4\_6\_3 \

w4\_7\_3 w4\_6\_4 \

w4\_7\_4 w4\_6\_5 \

w4\_7\_5 w4\_6\_6 \

w4\_7\_6 w4\_6\_7 \

w4\_7\_7 w4\_6\_8 \

w4\_7\_8) ece3663mult\_WT4

Adder0 (VDD VSS w4\_5\_0 w4\_4\_1 w4\_6\_0 w4\_5\_1 w4\_7\_0 w4\_6\_1 \

w4\_7\_1 w4\_6\_2 w4\_7\_2 w4\_6\_3 w4\_7\_3 w4\_6\_4 w4\_7\_4 w4\_6\_5 w4\_7\_5 \

w4\_6\_6 w4\_7\_6 w4\_6\_7 w4\_7\_7 w4\_6\_8 w4\_7\_8 \

OUT5 OUT6 OUT7 OUT8 OUT9 OUT10 OUT11 OUT12 OUT13 OUT14 OUT15 Cout) ece3663mult\_FA

ends ece3663multiplier

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*ALU Functions\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

myAdder (A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 B0 B1 B2 B3 B4 B5 B6 B7 B8 B9 B10 B11 B12 B13 B14 B15 AdderCarryin AdderCout AdderSum0 AdderSum1 AdderSum2 AdderSum3 AdderSum4 AdderSum5 AdderSum6 AdderSum7 AdderSum8 AdderSum9 AdderSum10 AdderSum11 AdderSum12 AdderSum13 AdderSum14 AdderSum15 VDD VSS) Adder\_16b m=1

mySubtractor (A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 B0 B1 B2 B3 B4 B5 B6 B7 B8 B9 B10 B11 B12 B13 B14 B15 SubtractorCout SubtractorSum0 SubtractorSum1 SubtractorSum2 SubtractorSum3 SubtractorSum4 SubtractorSum5 SubtractorSum6 SubtractorSum7 SubtractorSum8 SubtractorSum9 SubtractorSum10 SubtractorSum11 SubtractorSum12 SubtractorSum13 SubtractorSum14 SubtractorSum15 VDD VSS) Subtractor\_16b m=1

myAND (A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 B0 B1 B2 B3 B4 B5 B6 B7 B8 B9 B10 B11 B12 B13 B14 B15 VDD VSS AndOut0 AndOut1 AndOut2 AndOut3 AndOut4 AndOut5 AndOut6 AndOut7 AndOut8 AndOut9 AndOut10 AndOut11 AndOut12 AndOut13 AndOut14 AndOut15) ece3663AND\_16b m=1

myOR (A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 B0 B1 B2 B3 B4 B5 B6 B7 B8 B9 B10 B11 B12 B13 B14 B15 VDD VSS OrOut0 OrOut1 OrOut2 OrOut3 OrOut4 OrOut5 OrOut6 OrOut7 OrOut8 OrOut9 OrOut10 OrOut11 OrOut12 OrOut13 OrOut14 OrOut15) ece3663OR\_16b m=1

myPASSA (A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 VDD VSS PassAOut0 PassAOut1 PassAOut2 PassAOut3 PassAOut4 PassAOut5 PassAOut6 PassAOut7 PassAOut8 PassAOut9 PassAOut10 PassAOut11 PassAOut12 PassAOut13 PassAOut14 PassAOut15) ece3663PASSA\_16b m=1

myShifter (B0 B1 VSS VDD A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 ShifterOut0 ShifterOut1 ShifterOut2 ShifterOut3 ShifterOut4 ShifterOut5 ShifterOut6 ShifterOut7 ShifterOut8 ShifterOut9 ShifterOut10 ShifterOut11 ShifterOut12 ShifterOut13 ShifterOut14 ShifterOut15) shifter m=1

myMult (VDD VSS A0 A1 A2 A3 A4 A5 A6 A7 B0 B1 B2 B3 B4 B5 B6 B7 \

MultCout MultOut0 MultOut1 MultOut2 MultOut3 MultOut4 MultOut5 MultOut6 MultOut7 MultOut8 MultOut9 MultOut10 MultOut11 MultOut12 MultOut13 MultOut14 MultOut15) ece3663multiplier

//arbitrary function

//outs ArbitOut0 - ArbitOut15

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*Muxs\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

myMux0 (AdderSum0 SubtractorSum0 ShifterOut0 AndOut0 OrOut0 PassAOut0 MultOut0 Out0 VDD VSS MuxOut0 S0 S1 S2) mux m=1

myMux1 (AdderSum1 SubtractorSum1 ShifterOut1 AndOut1 OrOut1 PassAOut1 MultOut1 Out1 VDD VSS MuxOut1 S0 S1 S2) mux m=1

myMux2 (AdderSum2 SubtractorSum2 ShifterOut2 AndOut2 OrOut2 PassAOut2 MultOut2 Out2 VDD VSS MuxOut2 S0 S1 S2) mux m=1

myMux3 (AdderSum3 SubtractorSum3 ShifterOut3 AndOut3 OrOut3 PassAOut3 MultOut3 Out3 VDD VSS MuxOut3 S0 S1 S2) mux m=1

myMux4 (AdderSum4 SubtractorSum4 ShifterOut4 AndOut4 OrOut4 PassAOut4 MultOut4 Out4 VDD VSS MuxOut4 S0 S1 S2) mux m=1

myMux5 (AdderSum5 SubtractorSum5 ShifterOut5 AndOut5 OrOut5 PassAOut5 MultOut5 Out5 VDD VSS MuxOut5 S0 S1 S2) mux m=1

myMux6 (AdderSum6 SubtractorSum6 ShifterOut6 AndOut6 OrOut6 PassAOut6 MultOut6 Out6 VDD VSS MuxOut6 S0 S1 S2) mux m=1

myMux7 (AdderSum7 SubtractorSum7 ShifterOut7 AndOut7 OrOut7 PassAOut7 MultOut7 Out7 VDD VSS MuxOut7 S0 S1 S2) mux m=1

myMux8 (AdderSum8 SubtractorSum8 ShifterOut8 AndOut8 OrOut8 PassAOut8 MultOut8 Out8 VDD VSS MuxOut8 S0 S1 S2) mux m=1

myMux9 (AdderSum9 SubtractorSum9 ShifterOut9 AndOut9 OrOut9 PassAOut9 MultOut9 Out9 VDD VSS MuxOut9 S0 S1 S2) mux m=1

myMux10 (AdderSum10 SubtractorSum10 ShifterOut10 AndOut10 OrOut10 PassAOut10 MultOut10 Out10 VDD VSS MuxOut10 S0 S1 S2) mux m=1

myMux11 (AdderSum11 SubtractorSum11 ShifterOut11 AndOut11 OrOut11 PassAOut11 MultOut11 Out11 VDD VSS MuxOut11 S0 S1 S2) mux m=1

myMux12 (AdderSum12 SubtractorSum12 ShifterOut12 AndOut12 OrOut12 PassAOut12 MultOut12 Out12 VDD VSS MuxOut12 S0 S1 S2) mux m=1

myMux13 (AdderSum13 SubtractorSum13 ShifterOut13 AndOut13 OrOut13 PassAOut13 MultOut13 Out13 VDD VSS MuxOut13 S0 S1 S2) mux m=1

myMux14 (AdderSum14 SubtractorSum14 ShifterOut14 AndOut14 OrOut14 PassAOut14 MultOut14 Out14 VDD VSS MuxOut14 S0 S1 S2) mux m=1

myMux15 (AdderSum15 SubtractorSum15 ShifterOut15 AndOut15 OrOut15 PassAOut15 MultOut15 Out15 VDD VSS MuxOut15 S0 S1 S2) mux m=1

//for Cout bits

//passes AdderCout if adder selected, SubtractorCout if subtractor selected, multcout if mult,and VSS if anything else if selected

myMux16 (AdderCout SubtractorCout VSS VSS VSS VSS MultCout VSS VDD VSS MuxCout S0 S1 S2) mux m=1

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*Registers\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

myRegisterOut (VDD VSS CLK MuxOut0 MuxOut1 MuxOut2 MuxOut3 MuxOut4 MuxOut5 MuxOut6 MuxOut7 MuxOut8 MuxOut9 MuxOut10 MuxOut11 MuxOut12 MuxOut13 MuxOut14 MuxOut15 Out0 Out1 Out2 Out3 Out4 Out5 Out6 Out7 Out8 Out9 Out10 Out11 Out12 Out13 Out14 Out15) ece3663Register\_16b m=1

myRegisterA (VDD VSS CLK Ain0 Ain1 Ain2 Ain3 Ain4 Ain5 Ain6 Ain7 Ain8 Ain9 Ain10 Ain11 Ain12 Ain13 Ain14 Ain15 A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15) ece3663Register\_16b m=1

myRegisterB (VDD VSS CLK Bin0 Bin1 Bin2 Bin3 Bin4 Bin5 Bin6 Bin7 Bin8 Bin9 Bin10 Bin11 Bin12 Bin13 Bin14 Bin15 B0 B1 B2 B3 B4 B5 B6 B7 B8 B9 B10 B11 B12 B13 B14 B15) ece3663Register\_16b m=1

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*Buffers\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

clkbuff1 (VDD1 VSS1 clkIn asdaf) Inverter m=1000

clkbuff2 (VDD1 VSS1 asdaf CLK) Inverter m=1000

InvLoad0 (VDD1 VSS1 Out0 LoadOut0) Inverter m=8000/16

InvLoad1 (VDD1 VSS1 Out1 LoadOut1) Inverter m=8000/16

InvLoad2 (VDD1 VSS1 Out2 LoadOut2) Inverter m=8000/16

InvLoad3 (VDD1 VSS1 Out3 LoadOut3) Inverter m=8000/16

InvLoad4 (VDD1 VSS1 Out4 LoadOut4) Inverter m=8000/16

InvLoad5 (VDD1 VSS1 Out5 LoadOut5) Inverter m=8000/16

InvLoad6 (VDD1 VSS1 Out6 LoadOut6) Inverter m=8000/16

InvLoad7 (VDD1 VSS1 Out7 LoadOut7) Inverter m=8000/16

InvLoad8 (VDD1 VSS1 Out8 LoadOut8) Inverter m=8000/16

InvLoad9 (VDD1 VSS1 Out9 LoadOut9) Inverter m=8000/16

InvLoad10 (VDD1 VSS1 Out10 LoadOut10) Inverter m=8000/16

InvLoad11 (VDD1 VSS1 Out11 LoadOut11) Inverter m=8000/16

InvLoad12 (VDD1 VSS1 Out12 LoadOut12) Inverter m=8000/16

InvLoad13 (VDD1 VSS1 Out13 LoadOut13) Inverter m=8000/16

InvLoad14 (VDD1 VSS1 Out14 LoadOut14) Inverter m=8000/16

InvLoad15 (VDD1 VSS1 Out15 LoadOut15) Inverter m=8000/16